Determination of yield bounds prior to routing *

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Abstract

Integrated Circuit manufacturing complexities have resulted in decreasing product yields and reliabilities. This process has been accelerated with the advent of very deep sub-micron technologies coupled with the introduction of newer materials and technologies like copper interconnects, silicon-on-insulator and increased wafer sizes. The need to improve product yields has been recognized and currently some yield enhancement techniques are used in industry CAD tools. Still, the significant increase in problem size implies that considerable time and effort can be saved if the designer could predict the yield of each design stage.

In this paper we undertake an effort to derive bounds on the yield of the routing for a given placement. When the design is routed, resulting in a yield which is significantly smaller than the bound, the designer can choose to change the router cost functions, modify the placement or even re-design the unit in an attempt to increase the yield.

We compare the bounds on yield obtained for a set of standard benchmarks against exact yield values for the "vanilla" routings, and the run times needed to calculate the two. The results indicate that reasonably good estimates of yield can be obtained in significantly lower amounts of run time. The accuracy of the estimates increases when larger designs are considered as the simplifying assumptions made in the model no longer influence the estimates significantly.

1: Introduction

The need to improve product yields has been an important problem facing the semiconductor manufacturing industry [1]. Traditional yield models have focussed on the wafer yields as a function of defect densities, defect clustering and die area [1, 2, 3]. With his pioneering effort, Stapper showed that some of the yield detractors are influenced by how a design is laid out [2]. Based on this observation, substantial work [7] has been done to introduce the yield as a secondary objective to the traditional objectives of minimizing area and improving performance of designs. Most of the work [4, 5, 6, 8] has focused on developing efficient yield estimation and enhancement techniques. These approaches are widely used in the industry and have helped improve manufacturability significantly. Unfortunately, instead of being able to identify the actual cause of the yield detractors, the above efforts minimize the effects on product yields due to the design style being used. The next section attempts to motivate the need for alternative approaches to help locate the cause of yield degradation due to the design methodology used.

2: Motivation

One of the factors that influence the magnitude of yield detractors is the design methodology being adopted to create a design. A typical layout synthesis design flow comprises of several sub-stages like floorplanning, placement, routing, and compaction. Since most of these stages (except

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for layout compaction and routing) are far removed from the actual layout, forecasting yield values associated with each stage has not been attempted before. However, it would be useful to identify the amount of yield degradation introduced at each stage of the layout synthesis and spend more effort tuning these stages. It has been found that the routing is the most significant yield detractor given the large area it occupies and the large density of interconnects (resulting from the placement's objective to minimize total wire-length and area). Attempts to incorporate yield enhancement into the routing stage are being made at present. However, since the routing stage is time consuming and routability is influenced by the placement achieved, it would be useful if the designer could derive a bound on the yield of the routing. The designer can use this information to determine whether to perturb the placement stage (by modifying the placement cost function to incorporate yield costs) or to modify the router's cost functions to try and route the design to improve yield. In this paper we do not discuss how the placement can be perturbed to factor in the yield costs. However, we provide examples of how reasonably accurate yield bounds can be derived and used to aid determining whether or not to route the design with different wiring cost functions in order to improve yield. This paper also motivates the need for early yield estimation in order to have a better idea as to the profitability of manufacturing the design. If the yield estimates indicate very low yields, then significant design changes may have to be made in order to enhance manufacturability. Since the estimate can be obtained very quickly, it does not add a significant overhead to the design turn around time. In the next section we present the model we use to derive bounds on the yield prior to routing.

3: Bounds on yield for routing

We first list the assumptions used in our analysis. We assume that a designer has completed the placement step and has identified rectangular "channels" (as illustrated by Figure 1) that are to be the routing regions. The assumptions that apply to a gridded, channel routing problem with respect to wiring plane directions and fixed terminal locations hold. We assume that the wires are all of the same width. We ignore the vertical constraints between horizontal segments, since it is not our aim to identify a valid routing solution, but rather to derive a bound on routing yields. This implies that we deal only with the optimal assignment of horizontal segments to tracks (vertical segments connect to fixed terminals and we cannot control their yield by re-assigning them to different vertical tracks).

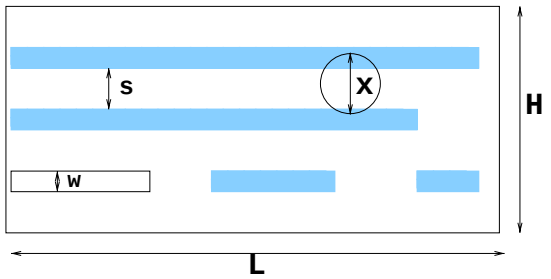

Figure 1. A channel having horizontal segments placed on fixed tracks

Stapper [2] studied defects in integrated circuit photolithographic patterns and presented expressions for the open-circuit and short-circuit critical area for N parallel conductors of length L. A_O, the open-circuit critical area of N parallel conductors of length L, averaged over all diameters x of

the defects (see Figure 1), is given by

$$A_O = \frac{L \cdot {X_O}^2 \cdot (N \cdot s + (N+1) \cdot w)}{2w \cdot (2w + s)} \tag{1}$$

where L is the length of a conductor, N is the number of conductors in parallel, X_0 is the defect diameter of the smallest observable defect, s is the minimum spacing between the conductors and w is the minimum width of the conductors.
Similarly, the short-circuit critical area of N parallel conductors of length L, denoted by A_S, is given by

$$A_S = \frac{L \cdot {X_0}^2 \cdot (N \cdot s + (N-1) \cdot w)}{2s \cdot (2s + w)} \tag{2}$$

For the purposes of our model we assume that we have m wiring levels for routing and n channels to route in the design. Also, we are provided with the open-circuit defect density D_O and the short-circuit defect density D_S. The average number of faults for level i is given by

$$\lambda_i = D_O \cdot \sum_{j=1}^{n} A_O^{(i,j)} + D_S \cdot \sum_{j=1}^{n} A_S^{(i,j)} \qquad (i = 1, ..., m) \tag{3}$$

where $A_O^{(i,j)}$ ($A_S^{(i,j)}$) is the open (short)-circuit critical area for the j^{th} channel in wiring level i. The overall yield for wiring level i, Y_i, is given by the negative binomial model [3]

$$Y_i = Y_o^{(i)} \cdot \left(1 + \frac{\lambda_i}{\alpha_i}\right)^{-\alpha_i} \tag{4}$$

where α_i is the clustering parameter and $Y_o^{(i)}$ is the gross yield factor for level i.
Assuming statistical independence among the m wiring levels, the overall yield (Y) over all the wiring levels can be calculated as

$$Y = \prod_{i=1}^{m} Y_i \tag{5}$$

The next section presents the algorithm used to obtain a near optimal assignment of horizontal segments to tracks so as to distribute the horizontal segments uniformly across all tracks and wiring levels. We proceed to derive expressions for $A_O^{(i,j)}$, $A_S^{(i,j)}$, and λ_i .
Denote:
$H^{(j)}$ - the height of channel j.
$N_i^{(j)}$ - the number of tracks in wiring level i (using minimum width and spacing rules) in channel j.
s_i - the minimum spacing rule for wiring level i.
w_i - the minimum width of conductors for wiring level i.
$s_i'^{(j)}$ - the new inter-track spacing for channel j, based on distributing segments uniformly in the channel, at wiring level i.
$u_i{}^{(j)}$ - the number of used tracks (i.e., number of tracks which contain a horizontal segment) in channel j, level i.
$a_i{}^{(j)}$ - the number of still available tracks (i.e., number of tracks to which no horizontal segments have been assigned) in channel j, level i.
The total number of tracks $N_i^{(j)}$ on wiring level i in channel j is given by

$$N_i^{(j)} = \lfloor \frac{H^{(j)} - s_i}{s_i + w_i} \rfloor \tag{6}$$

If ${u_i}^{(j)} + {a_i}^{(j)} = N_i^{(j)}$ and ${a_i}^{(j)} = 0$, then $s_i^{\prime(j)} = s_i$. If ${u_i}^{(j)} + {a_i}^{(j)} = N_i^{(j)}$ but ${a_i}^{(j)} \neq 0$, we can obtain the value of $s_i^{\prime(j)}$ as follows

$$s_i^{\prime(j)} = \frac{H^{(j)} \; - \; (u_i^{(j)} \cdot w_i)}{{u_i}^{(j)} - 1} \tag{7}$$

We then find the average length $L_i^{(j)}$ for the conductors in channel j, wiring level i. Having obtained the new spacing $s_i^{\prime(j)}$ and the number of parallel conductors in channel j and wiring level i, we can calculate the corresponding open-circuit critical area as follows

$$A_O^{(i,j)} = \frac{L_i^{(j)} \cdot {X_0}^2 \cdot (N_i^{(j)} \cdot s_i^{\prime(j)} + (N_i^{(j)} + 1) \cdot w_i)}{2w_i \cdot (2w_i + s_i^{\prime(j)})} \tag{8}$$

Similarly, we calculate the short-circuit critical area for channel j by

$$A_S^{(i,j)} = \frac{L_i^{(j)} \cdot {X_0}^2 \cdot (N_i^{(j)} \cdot s_i^{\prime(j)} + (N_i^{(j)} - 1) \cdot w_i)}{2s_i^{\prime(j)} \cdot (2s_i^{\prime(j)} + w_i)} \tag{9}$$

The average number of faults λ_i in wiring level i is found using equation (3). If the designer seeks to increase the accuracy of the bounds, he/she can add the average number of faults in the macro blocks to the average number of faults in the channels so as to account for the faults in the entire design. For the purposes of this model however, we restrict ourselves to faults in the channels only. In order to focus on channels whose yield values are significantly lower than the predicted bounds, our model also provides the yield bounds for individual channels. The average number of faults in level i of a channel j is given by

$$\lambda_{i,j} = D_O \; \cdot \; A_O^{(i,j)} \; + \; D_S \; \cdot \; A_S^{(i,j)} \qquad (i = 1, ..., m) \tag{10}$$

$\lambda_{i,j}$ is now substituted in (4) and then in (5) to obtain the yield for channel j across all the wiring levels. The algorithm is presented in the next section along with run time analysis.

4: Algorithm

This algorithm is applied to the inputs of an m-layer channel router to determine the bounds for the yield of the routing. The inputs to the algorithm include the net-list, routing channel geometry information, design rules, defect densities and defect clustering information for each wiring level.
The algorithm has two phases. The first phase consists of finding the lower bound on the number of wiring tracks needed given that the height of the channel is $H^{(i)}$ and that Z horizontal segments are to be assigned to the wiring tracks. Finding the lower bound on the number of tracks needed to assign all the horizontal segments is accomplished by finding "compatible" horizontal segments that can be placed on the same track. The Left Edge algorithm [9] is widely used to find the compatible sets of horizontal segments. This is equivalent to finding the minimum coloring for an interval graph (an interval graph represents each horizontal segment by a node and an edge connects two nodes whose segments have overlapping intervals). The Left-Edge algorithm first sorts the horizontal segments by their left coordinates. It then assigns one color at a time to as many segments as possible (by scanning the list of segments in ascending order and selecting those whose interval ranges do not overlap) before picking the next color. The algorithm yields a provably minimum coloring and has a time complexity of $O(ZlogZ)$ where Z is the number of horizontal segments in the channel.
The second phase of the algorithm proceeds to assign the segments to the tracks of the various wiring levels in a round-robin like fashion. The sum of the lengths of all the individual compatible segments for each track is found and the average net segment length L for each channel is obtained.

The assignment of segments to tracks is done trivially since the final yield bound is not concerned with the specifics of the segment placement in the tracks. If the number of compatible segments in a channel is C, then the second phase has a time complexity $O(C)$. The expressions in equations (6), (7), (8) and (9) are then used to obtain the critical area for each channel in a given wiring level. We repeat both phases of the algorithm over all the channels present in the design to obtain the critical area for all the channels in a given wiring level. Using defect density values, we use equation (3) to find the average number of faults in a given level. We can then use equation (4) to obtain the yield of a given wiring level and equation (5) to obtain the yield for the entire design. The algorithm is formally expressed in pseudo-code form below.

```
Begin
      for i = 1 to m {   // iterate over the wiring levels
        for j = 1 to n {   // iterate over the number of channels
           // n = Number of horizontal segments in j
           // C = Set of compatible horizontal segments
           // SC = Set of sorted compatible horizontal segments
           Read_Horizontal_Segments_from_Netlist (j);
           C(j) = LeftEdge (j,n);  Assign_To_Tracks (j,C);
           Compute_Average_Wiring_Length (i,j);
           Calculate critical area using eqns (6)-(9);
           Calculate average number of faults (i);
        }
        Y = Y * Calculate_Yield_Of_Wiring_Level (i);
     }
End;
```

5: Complexity Analysis

The time complexity of the algorithm is dependent on the run time of the Left Edge algorithm and the time taken to sort the compatible horizontal segments before assigning the same to various tracks. Let the number of horizontal segments present in channel j in wiring level i be $N^{(i,j)}$. The Left Edge algorithm takes $O(N^{(i,j)}logN^{(i,j)})$ time to form sets of compatible horizontal segments for this channel. Therefore, the Left Edge algorithm takes

$$T(m,n) = \sum_{i=1}^{m} \sum_{j=1}^{n} O(N^{(i,j)}logN^{(i,j)}) \tag{11}$$

time for a design having n channels and m wiring levels to route.
Let the number of compatible horizontal segments present in channel j in wiring level i be $K^{(i,j)}$. The time complexity of the second phase of the algorithm is $O(K^{(i,j)})$ since the segments are assigned to the tracks in a round robin like manner. By the very nature of the Left Edge algorithm such an assignment can be done without revisiting the segments. The assignment of compatible segments to the tracks is done in

$$T''(m,n) = \sum_{i=1}^{m} \sum_{j=1}^{n} O(K^{(i,j)}) \tag{12}$$

The Left Edge algorithm dominates the overall time complexity. Calculating the average wiring length in each level, the critical area for each level and the overall yield takes $O(1)$ time and therefore does not constitute a significant run time overhead. The above specified compute times are an improvement over the "vanilla" channel routers as our program ignores vertical constraints (resolving which is usually a time-intensive operation especially in the presence of cycles).

6: Numerical Results

The algorithm described in the previous section was incorporated into the standard cell layout synthesis flow of OCTTOOLS [10]. The experiments used only one wiring level (metal-1) for horizontal wiring. The logic synthesis benchmarks (iscas and lgsynth91) were used to synthesize ten layouts.

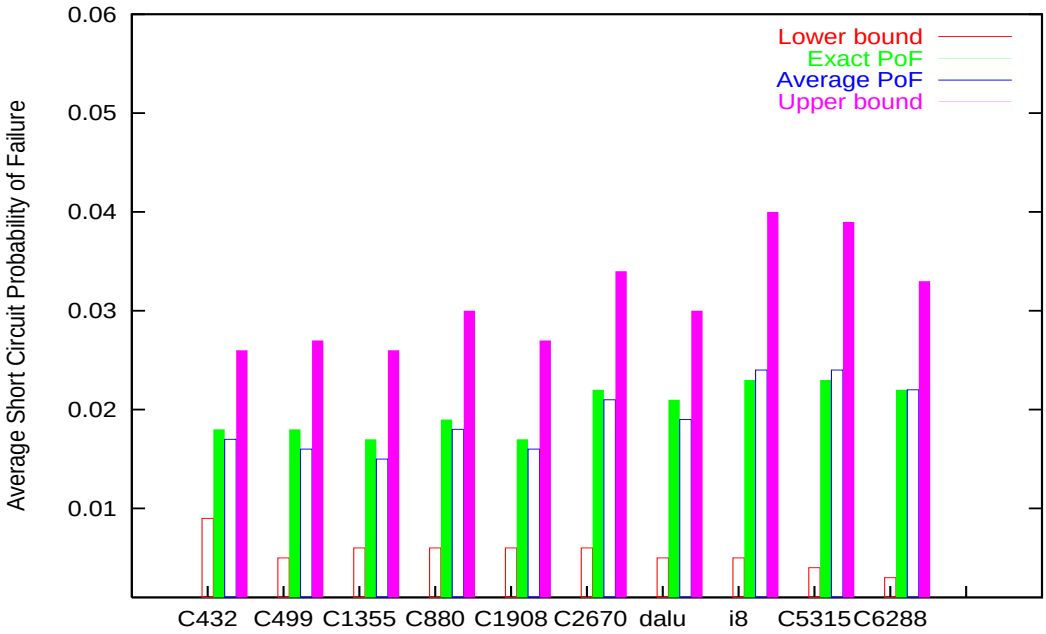

Figure 2. Short-Circuit Probability of Failure (POF) across the benchmarks

The Left Edge algorithm greedily assigns the segments to the tracks of the channel. The value of L for our purposes does not represent the length of the channel (the channel length will be equal to the length of the longest standard cell row making the critical area estimates much higher than actual values). Instead, L was computed as follows: The sum of the segments lying in each track of the channel was calculated. The track having the smallest(largest) length was used to generate the upper(lower) bound on the yield while the length of the segments averaged over all tracks was used to derive the average estimate. A correction factor was applied to the average estimate. Presence of vertical constraints in channel routing prevents otherwise compatible segments from being placed next to each other on the same track. This leads to increases in the inter-segment spacing seen in tracks of the routing channel. Since the model ignores vertical constraints the Left Edge algorithm tightly packs the segments in the channel as long as their horizontal constraints are not violated. The correction was done by adding the inter-segment spacing and dividing by the number of segments in the channel and deducting the same from the average estimate.
For each benchmark, we calculated the lower bound, the upper bound, and the average estimate, of the open- and short-circuit critical areas. These were then compared to the exact critical area values, generated using SCA/XLASER [6]. The corresponding probabilities of failure (where the probability of failure (POF) is defined as the ratio of the critical area to the total area of the design) are plotted in Figures 2 and 3. The average, over all benchmarks, of the percentage of difference between the average estimate and the exact POF, is -3.5% for short-circuit failures and -23.9%

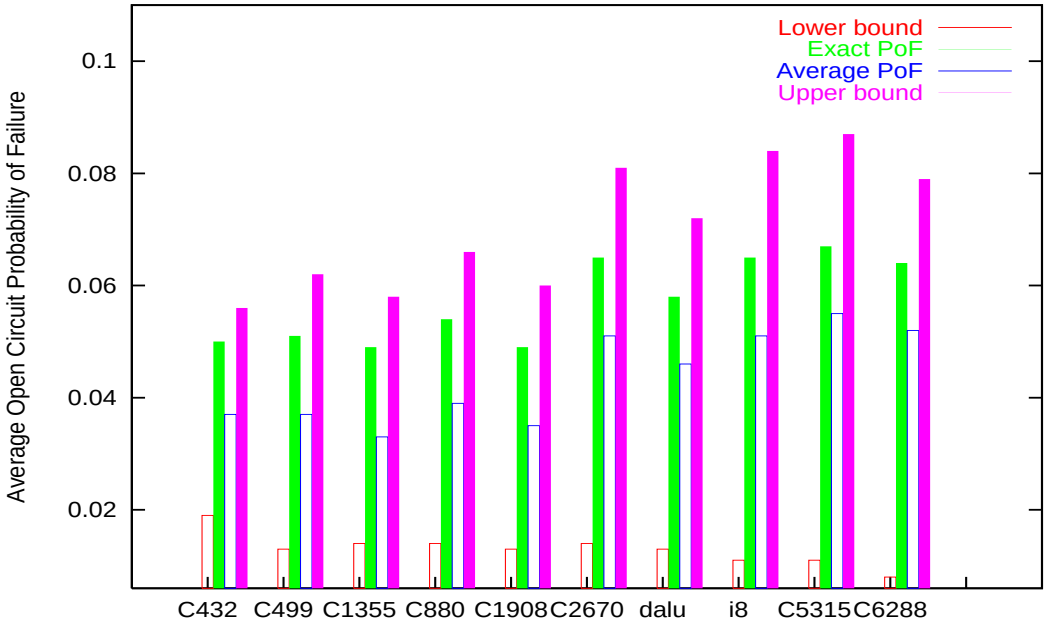

Figure 3. Open-Circuit Probability of Failure (POF) across the benchmarks

for open-circuit failures. Our model generates lower values of open-circuit POF as compared to the exact values because the vertical metal-1 wires created by the YACR routing tool are seen by SCA/XLASER but ignored by our model.

We then calculated the yield, for either open- or short-circuit failures, based on the three estimates and the exact values of the critical area. Figures 4 and 5 depict the yield as a function of the defect density for the largest benchmark example C6288 (the selected defect densities for shorts are an order of magnitude higher than for opens).

Table 1 shows that the run times for deriving the yield estimates are substantially lower then for performing exact computations.

Figure 6 illustrates the fact that the difference between estimated and actual yield is not affected

Benchmark Name	Number of Shapes	Accurate (secs)	Estimate (secs)
C432	8573	33.57	0.12
C499	9114	38.49	0.13
C1355	9481	39.65	0.13
C880	11058	47.48	0.15
C1908	11232	46.32	0.15
C2670	30602	151.70	0.69
dalu	32313	163.84	0.62
i8	33654	169.30	0.88
C5315	69241	374.49	1.94
C6288	123884	693.40	2.59

Table 1. Exact vs Estimated Yield calculation run times' comparison

by a change in the defect clustering parameter.
Figure 7 shows the exact and estimated yields for some of the benchmarks using a defect density of 120 per cm^2 and $\alpha = 2.0$. The difference in yields ranges between 1.0-4.0% for short-circuit failures, and between 0.4-4.0% for the open-circuit failures. It can be inferred that the simplifying assumptions made in the model do not skew the final results significantly in case of larger designs.

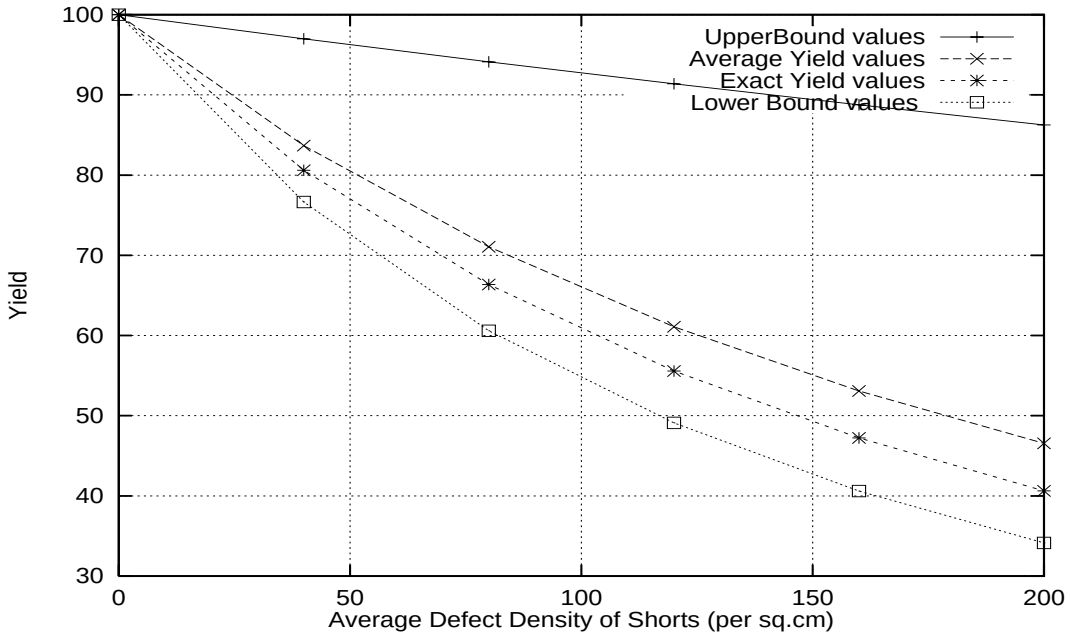

Figure 4. C6288: Exact vs Bounds on Short-Circuit Yields for $\alpha = 2.0$

7: Conclusion and Future Work

The experiments reinforced our belief that reasonably good yield estimates can be obtained in a fraction of the time needed for accurate yield calculation. It also helped motivate the need to make these estimates early on in the design so as to incorporate DFM techniques into the design flow rather than as an afterthought.
As a part of the future work, we would like to extend this approach to the area routing model. In addition, we would like this model to be used in the placement stage of an experimental design flow whose secondary objective of maximizing yield will be driven by the yield estimates.

8: Acknowledgements

The authors wish to acknowledge the important suggestions of Dr. Zahava Koren during the initial discussions on this work. The first author wishes to thank Dr. John Cohn, IBM EDA, for his guidance and encouragement.

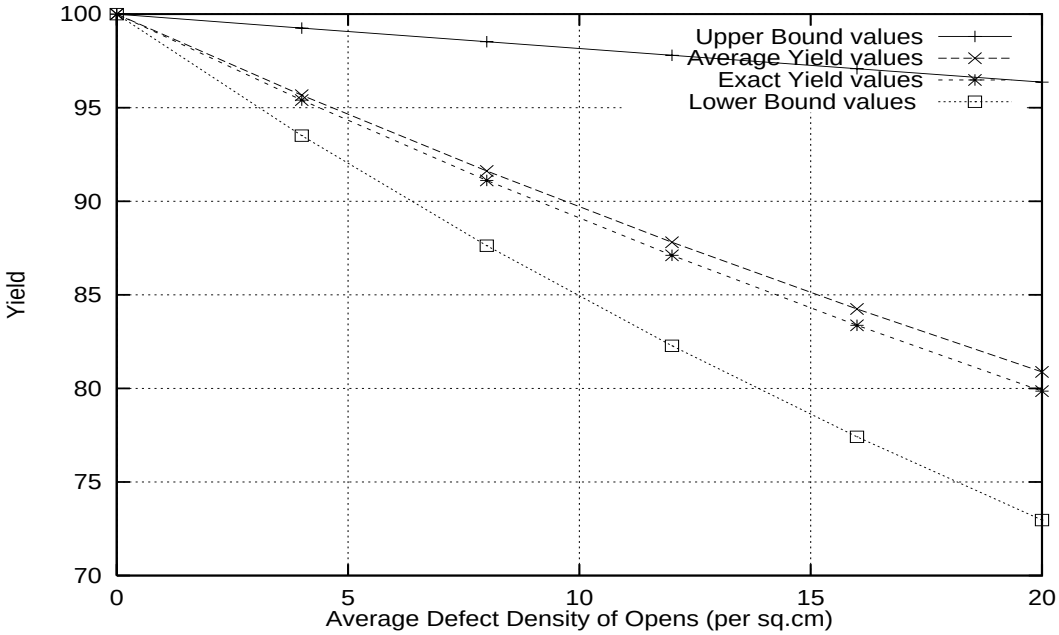

Figure 5. C6288: Exact vs Bounds on Open-Circuit Yields for $\alpha = 2.0$

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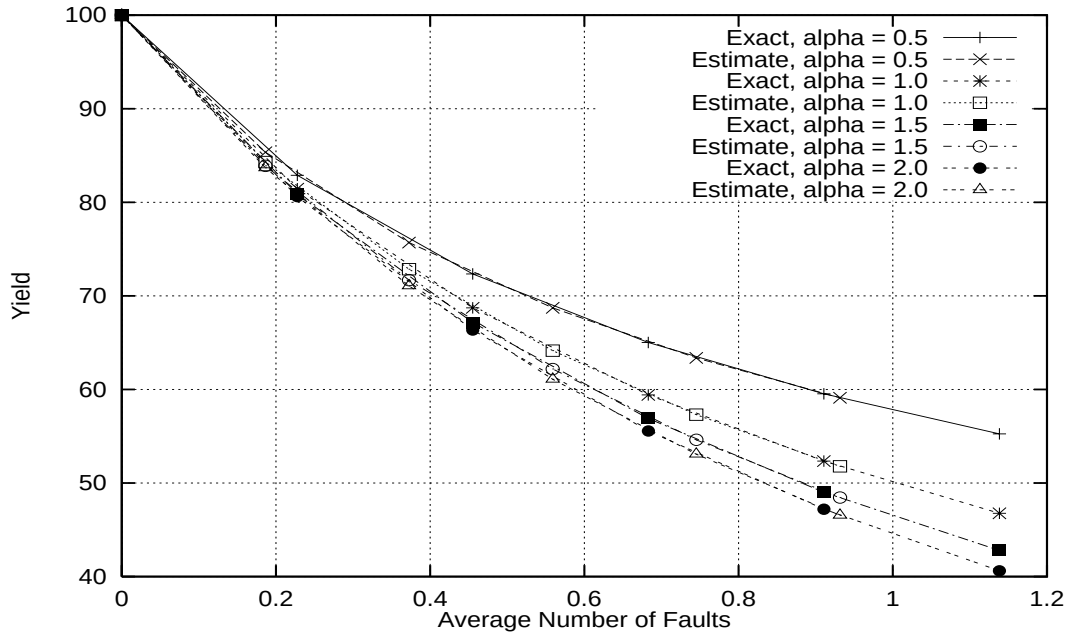

Figure 6. C6288: Exact vs Estimated Short-Circuit yields for various values of α

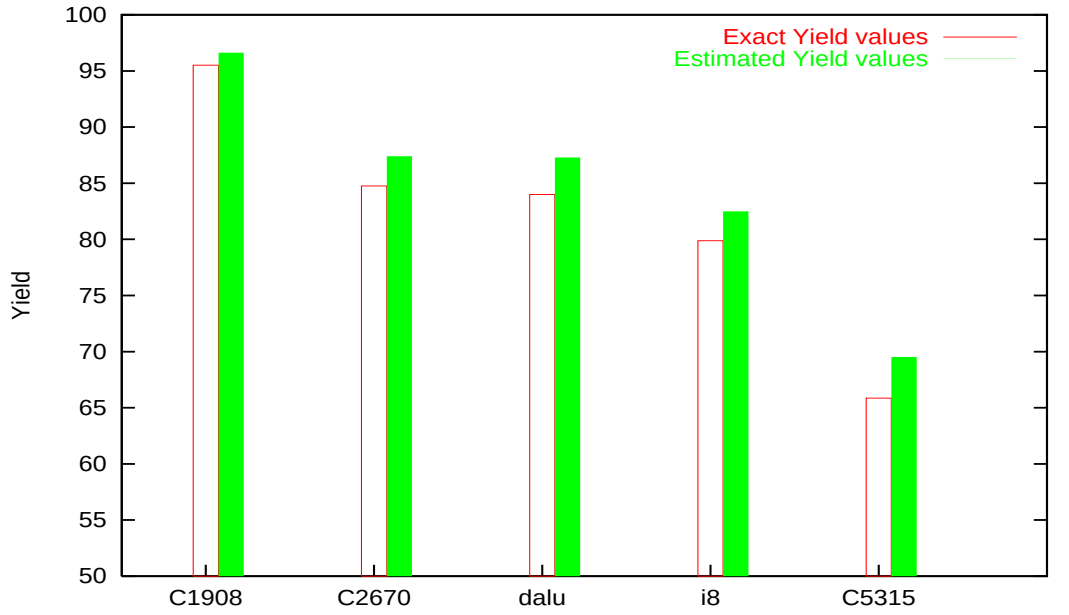

Figure 7. Exact vs Estimated Short-Circuit yields for $\alpha = 2$, $\lambda = 120$ def / cm^2