Yield Enhanced Routing for High-Performance VLSI Designs

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ABSTRACT

It is widely recognized that interconnects will be the main bottleneck in enhancing the performance of future deep sub-micron VLSI designs. Interconnects do not "scale" well with decreasing feature sizes and therefore dominate the delays in the integrated circuit. In addition to RC delays, crosstalk noise also contributes significantly to the delays experienced by a signal. Interconnects are more susceptible to manufacturing defects and therefore affect the product yields significantly. Recently, several channel-routing based solutions have been proposed to minimize crosstalk noise and also enhance yield of the routing. While these approaches are effective, they do not provide maximum benefits as they are either constrained by a particular design methodology or are post-routing steps which have limited scope for significant improvement. Also, design for manufacturability objectives have not been fully exploited by VLSI CAD tools as they do not integrate seamlessly into the conventional design flow and the added overheads make it less attractive. In this paper, we propose a modified routing algorithm that maximizes yield and reduces crosstalk noise while using minimal area for the routing. The yield enhancement objective has been integrated into the routing phase as a preferred constraint (a constraint that will be satisfied only if the primary constraints of minimal area and wire length have been satisfied) and fits well into the conventional design flow. This enables the router to produce an output which provides maximum achievable critical area reduction for the given routing solution. Post-routing layout modification is also done with the objective of minimizing the interaction area between the interconnects by exploiting the gridless property of the router. The above algorithm is incorporated into GLITTER (the gridless, variable width channel router), and the results on channel-routing benchmarks are presented. These results show a significant reduction in the critical area achievable by using the proposed algorithm.

Keywords: Design for Manufacturability, Yield Enhancement techniques, Crosstalk Noise, Channel Routing, Critical Area reduction.

1. INTRODUCTION

The need to develop faster integrated circuits (ICs) has resulted in smaller feature sizes, increase in the number of devices on a chip and advances in packaging technologies. These advances have been made possible by the significant improvements in the manufacturing process technologies. The improvements to the manufacturing processes have been accompanied by a greater increase in fab setup cost and complexity. This increased complexity has meant that a slight perturbation of the fab process can lead to significant yield losses. In order to improve manufacturability, newer techniques have been developed to address specific yield detractor mechanisms in the fabrication process. It has been found that modifications to the design can help improve increase yields as some of the yield losses are closely related to the designed IC layout. Therefore, Design For Manufacturability (DFM) assumes a lot of significance and present day designers are taking these issues into account while developing newer designs. In order to help the designers in this endeavor, several CAD techniques have been proposed to modify the design to aid manufacturability with minimal impact on the area and performance of the design.

The reliability of an IC is also an important issue as there have been several instances where an operational but unreliable IC has caused the system to fail under stringent conditions. One of the primary issues in improving the reliability of an IC is maximizing the signal-to-noise ratio of critical signals in the design. This is important because incorrect values of these critical signals can force the IC to deviate from its expected functionality and at times cause

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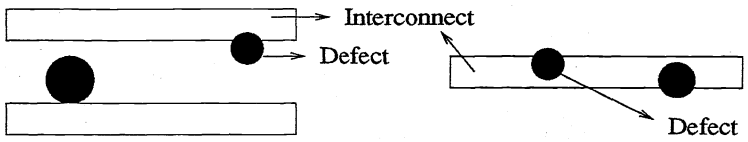

Figure 1. Not all defects cause a failure to occur.

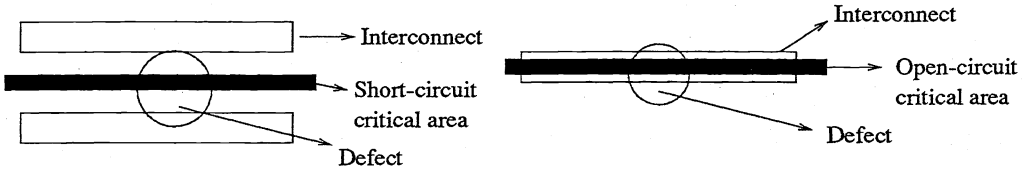

Figure 2. Defects falling on the "critical area" leading to failures.

the chip to fail. There are three sources of noise - reflection noise, switching noise and coupled noise. We consider coupled noise reduction issues in this paper as the cost function exhibits a strong dependence on the spacing between nets, which is similar to that of the critical area of short-circuit type failures' cost function. Coupled noise occurs between adjacent signal lines, when the driver switching in one net causes noise to be induced on the adjacent nets. The coupled noise also called "crosstalk" is to be minimized without increasing the area of the circuit.
In this paper, a new yield enhancement technique is presented as applied to the channel routing problem and the gains achievable in minimizing critical area and crosstalk noise while satisfying the primary objective of using minimal routing area is demonstrated. The rest of this paper is organized as follows. Section 2 presents a brief overview of the relationship between a designed layout and its yield and also crosstalk noise. Section 3 presents an overview of the existing yield enhancement and crosstalk minimization approaches and discusses some of their drawbacks. Section 4 outlines the approach taken in this paper and the benefits of the same. Section 5 discusses some of implementation details of our method with emphasis on the features of the grid-less, variable width channel router GLITTER. Section 6 details the algorithm and presents optimality proofs. Section 7 highlights the results of experiments performed on the channel routing benchmarks and Section 8 concludes the paper with a brief list of the ongoing and future work.

2. NEED FOR DFM

In this section we describe the relationship between a laid out design and the yield of a manufactured IC. Stapper's work[1,2] was the first effort at identifying the link between a given design and its yield. He pioneered the development of the various yield models[3] and also formalized the defect-size distribution function, which has been the basis for most yield enhancement efforts. Critical area[4] is defined as the area in which a center of a defect must fall to cause a fail. When photolithographic defects are very small there is enough conductive material left to allow the lines to conduct currents without failure. The fact that *not all defects cause a failure to occur* is an important reason for using critical area modeling to detect highly defect-susceptible regions in a given design. This is illustrated in Figure 1. In Figure 2, the short circuit and open circuit critical areas are shown.

It is clear from the above figures that increasing the spacing between the shapes on a laid out design helps reduce critical area. But, since the area occupied by a design also has a significant impact on the wafer yield, the objective function for yield enhancement is that of reducing the total critical area without increasing the initial design area. This objective function has been used extensively to develop CAD tools that enhance yields of designs at various stages of the design flow. Yield enhancement techniques have been successfully prototyped in the compaction[5] and routing[6,7] stages of a typical design flow and newer techniques have been proposed for applying the same at the floorplanning stage.[8] But significant benefits are still achieved primarily through layout synthesis techniques[9] and therefore there is an increased focus on routing and compaction algorithms for enhancing manufacturability of a designed IC.
Early work at IBM[1,2] analyzed the pattern of manufacturing defects occurring for various fabrication technologies and derived an empirical model for the defect-size distribution function of a given fabrication technology. This distribution indicated that the probability of a defect of size X occurring decreases with increasing defect sizes as

$\frac{1}{X^3}$.This relationship is bulwark of layout-synthesis based yield enhancement as it helps identifying the critical areas of a given design by either deterministic shapes-based approach[10] or non-deterministic Monte-Carlo approach.[11] These yield estimation techniques calculate the total critical area as a sum of the critical areas weighted by the defect size distribution. This information is then used to obtain the cost of the new yield enhanced solution. If the yield enhanced solution has a lower total critical area, the layout modifications have enhanced the overall yield of the IC. The overall IC yield is given by the negative binomial distribution[3] as follows

$$Y = Y_o \cdot (1 + \frac{\overline{\lambda}}{\alpha})^{-\alpha} \tag{1}$$

where Y_o represents the gross yield factor, $\overline{\lambda}$ is the average number of faults per chip and α is the defect clustering parameter. The average number of faults per chip is calculated as a product of the total critical area and the density of defects per unit area. Therefore, it is essential to obtain critical area reduction if yield enhancement is to be achieved. The critical area reduction must be applied to all the layers of a design to maximize yield enhancement.
With advent of high-speed ICs, the effects of parasitics (capacitance and inductance) in an interconnect have begun to dominate.[12] This has meant that parametric yield losses on account of excessive crosstalk noise have increased. Therefore, reliability enhancement is important in high performance designs so as to offset the effects of the increased device speeds and decreased feature sizes. Crosstalk noise minimization is important to ensure that the signal integrity of "critical signals" (on adjacent nets) is not compromised. The crosstalk noise is dominated by the cross-coupling capacitance between adjacent nets[13] and is proportional to the net overlap length. Cross-coupling capacitance as a function of the adjacent net spacing is given by[14]

$$C_{coup} = \epsilon_{ox} \{ 1.93 (\frac{T}{H})^{1.1} + 1.14 (\frac{W}{H})^{0.31} \} (\frac{S}{H} + 0.51)^{-1.45} \tag{2}$$

where C_{coup} is the Cross-coupling capacitance, ϵ_{ox} is the dielectric constant of oxide, T is the thickness of interconnect wire, H is the thickness of the oxide, W is the width of the wire, S is the spacing between the wires. Therefore, in addition to reducing the net overlap, it is essential to increase the spacing between the nets in order to reduce cross-coupling capacitance and hence crosstalk noise.
It has been found that the interconnects dominate the yield losses because they typically account for 70% of the given IC area. Therefore, most of the yield enhancement techniques have focused on modifying interconnects to improve IC yields. The following section briefly describes the existing yield and reliability enhancement techniques focusing on the channel routing problem in particular. The above discussion clearly illustrates that the two cost functions of critical area reduction and crosstalk minimization are similar in behavior. It must however be noted that crosstalk minimization is applicable primarily to "noisy" nets (nets carrying critical signals having opposing transitions) while critical area reduction is applicable to all the nets irrespective of the signals that they carry. Also, a chip can fail even if the crosstalk noise on a single net exceeds its "noise-margin" but manufacturability is not affected significantly if a single net has a high susceptibility to short-circuit causing defects. The issue of the relationship between critical area reduction and crosstalk minimization and the need for trade-offs between the two objectives was addressed by A. Venkataraman et.al.[15] In this paper, the primary objective is maximizing critical area reduction by incorporating the yield enhancement objective seamlessly into the primary objective function of minimal area routing and we show that it also leads to a reduction in the crosstalk noise of nets having a significant cross-coupling capacitance.

3. EXISTING APPROACHES

As discussed earlier, the emphasis on the routing step for yield enhancement has been greater considering the fact that the interconnects are more susceptible to catastrophic fails as compared to other components of the IC. Existing work has focused on VLSI routing algorithms (grid-based channel routing algorithms in particular) and suggested metrics that account for critical area reduction and reduction of crosstalk noise. But most of these techniques have tended to post-process the design to enhance manufacturability and reliability with a view to ensuring that the primary constraint of minimal area routing remains unchanged. But IC designers disapprove of the post-processing step as it introduces some additional delays on the critical paths and forces them to iteratively re-check the design so as to make the performance match the initial specification. Also, post-processing involves having to redo the design verification checks as there always exists a possibility of a degenerate case in the design which can result in a design rule violation when a CAD tool modifies the design for DFM. Therefore, yield enhancement as a post-processing step

is not an attractive option as yet. To make yield enhancement attractive, it should be incorporated as a preferred constraint along with other primary constraints of conventional channel routing. This implies that the DFM issues will be addressed seamlessly along with conventional design issues using minimal overheads.

Most of the existing yield enhancement techniques have used "gridded channels"[6,7,16–18] so as to use a symbolic representation of the problem. This has meant that the suggested approaches apply only to particular methodologies and therefore their use has been restricted in practice. The primary drawback of the grid-based approach is that it is highly constrained by having to place nets on fixed track positions. As the track separation is usually determined by the via to via spacing (which is greater than the metal-metal spacing), the extra available space is not exploited and therefore maximum yield enhancement benefits are not achieved. In their work, Karri et.al[19] have suggested using simulated annealing based techniques to enhance the yields by reducing the adjacent net overlap, but this work was also constrained by the use of fixed tracks. In addition, the approach could not guarantee best results with respect to the critical area reduction as the optimization technique used is non-deterministic and therefore convergence to the global minima is not guaranteed. Other approaches have tried to emphasize on via-minimization[6] and also wire length minimization[20] as DFM objectives. Though our work does not explicitly address these issues, we expect our approach to hold good as the basic premise behind our approach is to satisfy primary objectives first and attempt to satisfy all the specified secondary objectives without degrading the primary objectives. Therefore, if the primary constraints are violated then the preferred constraints are ignored to satisfy the primary constraints, though every effort is made to satisfy preferred constraints in the event that such a solution exists. It is possible to assign weights to the various secondary objectives based on the characteristics of a given fabrication process so as to achieve a final yield enhanced solution. Increasing the number of secondary objectives to be considered does not yield significant improvements as the problem becomes highly constrained and the quality improves negligibly at the expense of increased computation cost.

In this paper, a gridless, variable width channel router is used to incorporate a simple yield enhancement algorithm that also provides reduction of crosstalk noise. The existing crosstalk minimization approaches except[21] mainly focus on grid-based channels and apply track permutations to minimize cross-coupling capacitances[22,23] between adjacent nets. But this has meant that the overall critical area reduction achieved was much lesser and the problem of not being able to exploit inter-net spacing to reduce cross-coupling capacitance remained. Also, the grid-based crosstalk minimization approaches do not consider critical area reduction and therefore the DFM objectives were not fully integrated into the conventional routing step.

4. OUTLINE OF OUR APPROACH

In order to avoid the drawbacks of existing approaches to yield enhancement, critical area reduction is implemented as a preferred constraint. This means that if there exists more than a single possible routing solution which leads to a minimal area routing, all feasible candidate solutions are evaluated for their total critical area and the solution having least critical area is selected. If the router requires an increase in area while considering the yield enhancement objective, the algorithm will reject this solution and instead keep the solution that is good with respect to routing area but poor with respect to manufacturability. This is because the IC yield varies as an inverse function of the design area and therefore an increase in design area can lead to reduced yield. Also, increased design area leads to increased wire lengths and this in turn increases the susceptibility to open-circuit causing defects. The approach taken by Huijbregts[7] in integrating the critical area reduction cost function into the routing step was to use the weighted critical area of each net (based on a given defect size distribution) as the cost function. This increases the accuracy at the expense of compute time overheads. In our approach, a simple metric is used to represent the extent of critical area between horizontal nets. The metric is given by

$$NW = OW + \frac{net \quad overlap}{maximum \quad net \quad overlap} \times OW \tag{3}$$

where NW represents the edge weight after considering net overlap and OW is the minimal edge weight as defined by the inter-net spacing rule. Ideally, nets with large overlap lengths would be spaced apart as much as possible. Since the weight associated with a net pair is large, the constraints in the graph are modified to reflect the required increase in the amount of separation between the nets. Therefore, the edge weights in the constraint graph are a function of the extent of the net overlap. Though this metric is very simple, it captures the property of having to separate by large distances nets with high short-circuit fault susceptibility. The next version of this tool will incorporate into

the cost function, the total critical area specified as critical areas weighted over the given defect size distribution. This would enable us to study the trade-offs between compute time versus achieved yield enhancement. Our current results indicate that the simple metric was sufficient to obtain significant improvements in the overall yield.
The gridless property of the router helped us exploit the inter-net spacings to separate out the nets based on the net overlaps with other horizontal nets. The nets having most overlap were therefore separated by the largest allowed distance and nets having lesser overlaps were placed adjacent to each other. Therefore, the long nets which have significant cross-coupling capacitances were separated and also "shielded" by nets having lesser cross-coupling capacitances. Therefore, the primary issues facing today's high performance designs - i.e., maximizing performance and increasing manufacturability and reliability are taken care of in our approach.

5. IMPLEMENTATION DETAILS

The yield enhancement algorithm was incorporated into the gridless, variable width channel routing tool called GLITTER.[24] GLITTER employs the constraint graph based formulation to depict the spacing constraints between the nets using the design rules specified by the user. The horizontal subnets are represented as nodes of the graph, and the constraints are represented as edges. Horizontal constraints between the subnets are represented as undirected edges while vertical constraints are represented as directed edges. If there are "cycles" in the graph, the cycles are first broken to convert the graph into an acyclic graph so that the Dijkstra's shortest path algorithm can be used to determine the lower bound for the channel height. If the user specified channel height was less than the lower bound, the router fails to complete the routing successfully. The maximum required channel height is computed based on the various boundary constraints and also the net to net constraints. This is the upper bound calculated by GLITTER to successfully complete the routing using minimal channel height. To find this upper bound, it is essential to resolve the directions assigned to the undirected edges (namely, the horizontal subnet constraints). Therefore, the problem can be formally stated as follows :
1. Assign directions to the undirected edges so that no cycles are formed in the graph.
2. Total weight of the maximum *weighted directed path* from the upper boundary to the lower boundary is minimized.
The above problem was solved earlier by H.Chen et.al[24] while developing GLITTER and obtained results that were comparable in run time and quality to that obtained by using other grid-based approaches. The performance of the algorithm is dependent on the heuristic employed to assign directions to the undirected edges of the constraint graph. The robustness of the edge selection heuristic made GLITTER an excellent candidate for implementing the yield enhancement objective. To incorporate yield enhancement, we had to consider the same problem as above except that any solution that increases the weight of the shortest directed path must not be accepted. This implies that in order to complete the routing using a minimal area, a solution that is poor with respect to manufacturability is obtained. But it also implies that if a solution that preserves the shortest directed path weight is obtained, then the yield enhancement achieved is most optimal for the given input. Therefore, assigning directions to the undirected edges of the constraint graph is very important in arriving at a good solution for maximal yield enhancement benefits also. If the user is not satisfied with the results of the heuristic algorithm, a simulated annealing technique is provided to search for the global optima using the local optima as a starting point. As the starting point of the iterative improvement scheme is good, it reduces the search time (otherwise, there is no guarantee that the iterative improvement approach will provide a better solution in a fixed time). In the next section we briefly outline the algorithm and analyze the performance issues from a compute time viewpoint.

6. ALGORITHM AND PERFORMANCE ANALYSIS

In this section we briefly outline the yield enhancement algorithm and provide arguments for the optimality of using the gridless, constraint graph based approach over the grid-based, exhaustive approach.

```
Yield Enhanced Routing()
{
  Build Constraint Graph using specified design rules;
  Detect and Remove Cycles;
  Calculate Net Overlap for all net pairs;
  Update edge weights to include extent of net overlap;
  for (all the undirected edges)
```

Assign directions to edges such that area is not increased;
}

The time complexity of the algorithm is of the order of $O(V^2 \times E)$ where V represents the number of vertices in the constraint graph and E represents the number of edges in the graph. The number of vertices V represents the number of horizontal subnets in the input and therefore the compute cost increases significantly with the increase in the number of distinct terminals to be routed. While building the constraint graph, redundant constraints are eliminated to make the solution more efficient with respect to run time. Therefore, E which represents the constraints (corresponding to the edges of the constraint graph) is kept as small as possible. The only overhead involves having to update the edge weights based on the net overlaps and this takes $O(E)$ time to accomplish. Since this is a one time compute step, this overhead is a negligible fraction of the overall run time. The most expensive step which dominates the computation complexity is the edge-selection algorithm which determines the directions to be assigned to undirected edges. The cost of this step does not vary with the incorporation of the yield enhancement objective function. For each edge, it takes $O(V^2)$ time to update the weights associated with its directed path. Therefore, it takes $O(V^2 \times E)$ to update the weighted directed acyclic constraint graph. The time complexity of the yield enhancement algorithm is therefore of the same order as the channel routing algorithm and for negligible compute time overhead, the yield can be significantly improved.
The grid-based approaches for crosstalk noise minimization have used the mixed Integer Linear Programming formulation[22] which is very compute intensive. The yield enhancement approach suggested by Karri et.al[19] is based on the non-deterministic simulated annealing approach and therefore is very inefficient with respect to run-time in addition to not being able to guarantee an optimal solution. The post-routing yield enhancement technique proposed by Waring et.al[18] does not provide details of the run-time overheads associated with incorporating yield enhancement. However, a preliminary analysis of their approach indicates that the steps for identifying tracks that can be fully displaced and that of identifying the possible candidates for corner flipping (since this step involves having to ensure that there is no increase in the wire-length) involve a significant search overhead. Similarly, the previous work by Kuo[6] does not provide details of the added cost in incorporating yield enhancement into their objective functions. Our approach makes a strong argument for incorporating the yield enhancement objective function into conventional design flow steps and also for using simpler metrics to discern solutions that enhances DFM without degrading the primary objectives.

7. RESULTS

The above algorithm was run on the standard channel routing benchmarks and the results validated the claim that it was possible to incorporate yield enhancement objectives into the traditional objectives of minimal area routing and achieve benefits of reduced total critical area and crosstalk noise. Table 1 shows some of the results of our algorithm on the example benchmarks. We have used Metal-1 layer for horizontal subnets and Metal-2 layer for vertical subnets. Since the Metal-2 layer is constrained to be connected to a fixed terminal on either the top or bottom of the channel, our approach does not modify Metal-2 layer for yield enhancement. Therefore, the achievable yield enhancement was based on the reduction in critical area of Metal-1 short circuit type failures. Since the routing area was not increased, we have used the average number of Metal-1 short circuit failures (weighted over the entire defect-size distribution) as an indicator of the yield of the channel routing. This figure of merit ($\overline{\lambda}$) is obtained as a sum of the product of the Probability of Failures (POFs) and defect densities (for all the defect sizes) and its relation to yield is shown in Equation 1. The first column in Table 1 shows the benchmark names.[25] The next column specifies the average number of Metal-1 short circuit type failures for the original routing. The third column specifies the average number of Metal-1 short circuit type failures for the routing using yield enhancement as a preferred constraint. The last column shows the achieved reduction in the average number of Metal-1 short circuit type failures. The results clearly show that using the preferred constraint, gridless channel router helped reduce the short circuit fails' critical area over the entire range of defect sizes without having to increase the area of the channel. The difference in run times before and after incorporating the yield enhancement objective was insignificant for all the benchmarks except the Deutsch Difficult example for which a one second increase was recorded. The simulated annealing approach did not provide significant improvements as compared to the heuristic method and the run times were several orders of magnitude larger. Two examples of the routing before and after yield enhancement are illustrated in Figures 3, 4

and Figures 6, 7 respectively. The plots showing the original and new probability of failures for various defect-sizes are also shown in Figure 5 and Figure 8 respectively.

Examples	Average number of short circuit fails (original routing)	Average number of short circuit fails (yield enhanced routing)	Percentage reduction in number of short circuit fails
Example1	0.003952	0.003382	14.2
Example2	0.004621	0.003826	17.2
Example3	0.004020	0.003577	11.0
ex1[25]	0.006112	0.005984	2.0
ex3b[25]	0.005574	0.005243	6.0
ex3c[25]	0.006015	0.004963	17.5
Diff. Ex[25]	0.005507	0.004822	12.4

Table 1. Experimental results

8. CONCLUSION AND FUTURE WORK

The results clearly show reductions in the critical area and cross-coupling capacitance of the nets in the routing. In addition, the negligible increase in run times validated the use of a simpler metric to direct the yield enhancement algorithm. Though the simulated annealing scheme did not provide significant improvements, increasing the number of iterations can help obtain better solutions. It also indicates that the heuristic used in GLITTER is relatively robust and therefore it might not be necessary to spend significantly more compute time for a negligible increase in the quality of the solution.

The focus of this paper was to illustrate the need to integrate the objectives of reliability and manufacturability into traditional approaches in the typical design flow. Future work includes modifying the yield enhancement cost function to include the defect size distribution function's influence on the solution. This will help study the trade-offs between increasing the complexity of the cost function against the loss in achievable yield enhancement by using a simpler metric. Ongoing work includes extending this concept to the detailed area-routing problem. As a part of the continuing effort to highlight the need to integrate the DFM objectives into the conventional flow, future work involves looking at the other steps of the design flow where such seamless integration of secondary objectives can be achieved.

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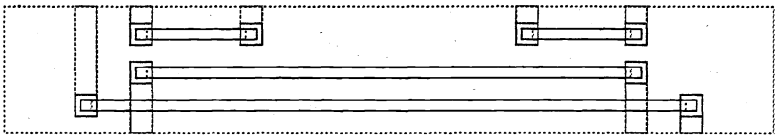

Figure 3. Example1 - Routing without considering yield enhancement.

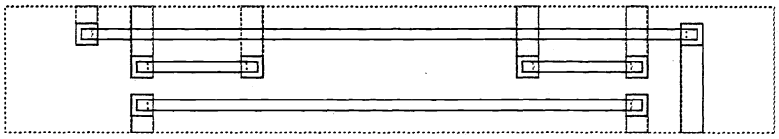

Figure 4. Example1 - Routing after considering yield enhancement as a preferred constraint.

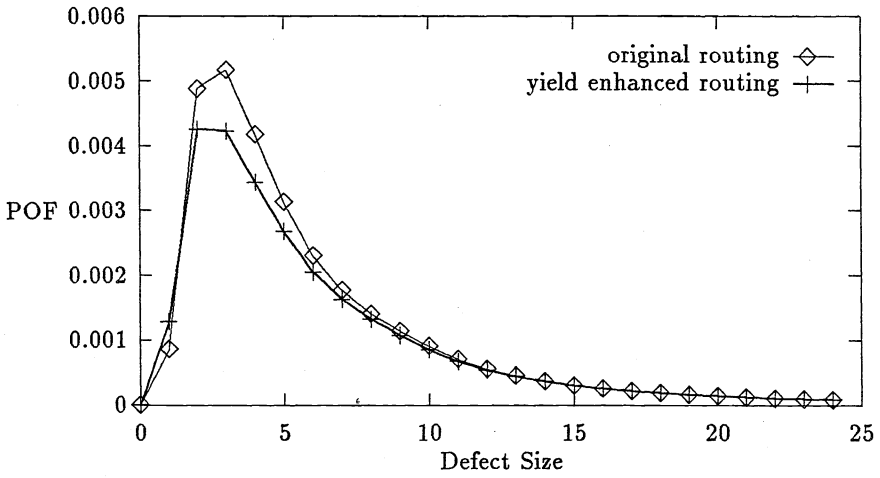

Figure 5. Example1 - Probability of Fails versus Defect-size

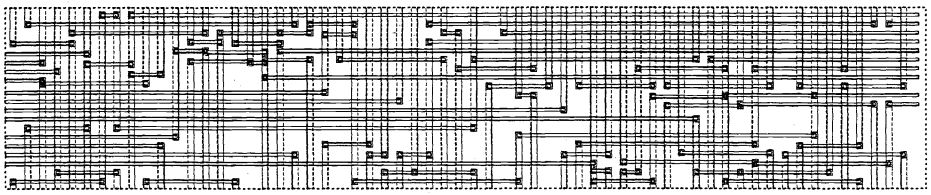

Figure 6. ex3b - Routing without considering yield enhancement.

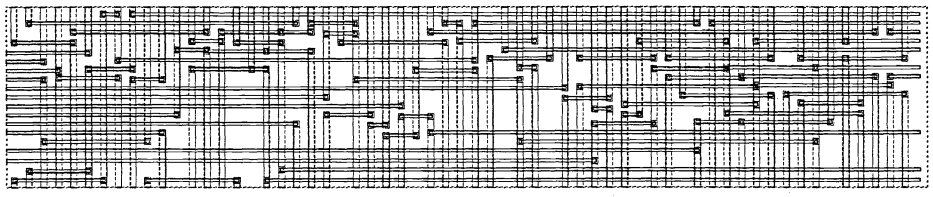

Figure 7. ex3b - Routing after considering yield enhancement as a preferred constraint.

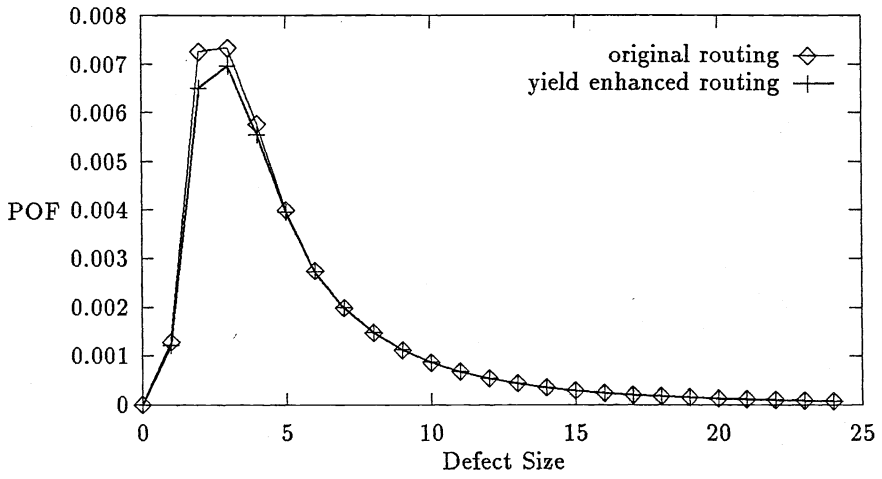

Figure 8. ex3b - Probability of Fails versus Defect-size