3-D Integration Requirements for Hybrid Nanoscale-CMOS Fabrics

Pavan Panchapakeshan[1], Priyamvada Vijayakumar[1], Pritish Narayanan[1], Chi On Chui[2], Israel Koren[1] and C.Andras Moritz[1]

[1]Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, MA 01003, USA
[2]Department of Electrical Engineering, University of University of California, Los Angeles, CA 90024, USA
Email:{ppanchapakesh, andras}@ecs.umass.edu

***Abstract* — Several nanoscale computational fabrics based on various physical phenomena have been proposed in recent years. However, their integration with CMOS has only received limited attention. In this paper we explore some of these integration challenges focusing on registration and the overlay between layers. We propose and evaluate a new 3D integration approach by carefully mixing standard CMOS design rules and nanoscale constraints. We address the following questions: (i) How much overlay precision is necessary? (ii) What is the impact on yield if different overlays are used?, and (iii) How can we mitigate the overlay requirements? For a nanoprocessor design implemented in N^{3}ASIC (a hybrid nanowire-CMOS fabric) we show that a 100% yield is achievable even for a today's known overlay of 3σ=±8nm (ITRS 2009). The N^{3}ASIC fabric version retains 6X density advantage compared to a projected 16nm CMOS scaled design even after 3D integration.**

Index Terms – 3-D integration, Mask overlay, alignment.

I. Introduction

Manufacturing of integrated nano-systems with sub-lithographic structures continues to pose significant challenges. While unconventional manufacturing techniques such as imprint lithography [1] and SNAP [2] can produce ultra-dense regular structures at sub-10nm features; alignment with respect to previously formed patterns is still a concern (overlay alignment for imprint lithography is 3σ =±105nm [3]). Photolithography on the other hand has excellent mask overlay but may not achieve the same density. In this paper we propose a hybrid nano-CMOS 3-D integration approach that combines the advantages of unconventional and conventional manufacturing processes. We discuss the overlay requirements for hybrid nanofabrics, and show how full 3-D integration may be achieved using standard CMOS design rules. We discuss how design choices and order of process can mitigate overlay and alignment requirements, while retaining density benefits of sub-lithographic processes.

II. 3-D Integration Requirements

Nanofabrication techniques based on contact patterning or self-assembly based approaches tend to favor the formation of regular periodic structures such as grids. Registration requirements in such regular structures are alleviated since an initial lithography mask may be 'offset' with no loss of functionality. For example, NASICs [4][5] is a 2-D nanowire grid based fabric which uses lithography masks for functionalization, contacts etc. It was observed that a yield of ~70% can be obtained for an overlay of 3σ=±5.7nm (Manufacturing solutions known – ITRS[6]). In this paper, we discuss how regular nanofabrics could be built with full 3-D integration, while addressing overlay requirements and density implications.

One approach to build a fully integrated 3-D fabric is to use only optical lithography for all process steps. While the overlay precision is projected to be excellent and yield very high, this approach is expected to have low density when compared to techniques that use self-assembly/ unconventional nanofabrication techniques.

A second approach would be to combine unconventional and conventional manufacturing flow to obtain a 3D integrated fabric of high density. Such an approach has been adopted in CMOL [7] and HP's FPNI [8] nanofabric, where unconventional techniques such as nanoimprint are necessary after the fabrication of CMOS layers. As mentioned previously, overlay alignment for imprint lithography is 3σ=±105nm [3], which implies significant challenges in alignment against previously formed features. Such a large overlay misalignment can contribute to significant yield loss (or conversely trading-off much of the density benefit for acceptable yield) and is not ideal.

Conventional CMOS manufacturing flow guarantees very high alignment and overlay precision but fails to realize a highly dense nanofabric. The unconventional nanomanufacturing techniques guarantee a highly dense fabric but have very poor alignment precision with respect to previously formed patterns. With this learning, we propose a nano-CMOS integration approach which considers the *order of manufacturing process steps* along with fabric design choices which aid in mitigating mask overlay while still achieving an ultra dense fabric.

It was seen that a uniform nanowire grid structure at the bottom implies that the first process step may be 'offset' with no loss of functionality. Furthermore, if an unconventional manufacturing step is performed before any lithographic masking, it is not affected by any overlay requirement. This fact motivates us to utilize the uniform nanowire grid as the bottommost layer in the 3-D integration approach. The regular structure mitigates the impact of mask offset while

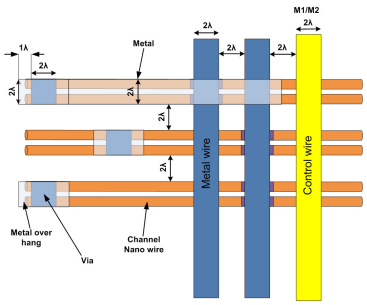

Fig.1 NW design rules for 3-D integration

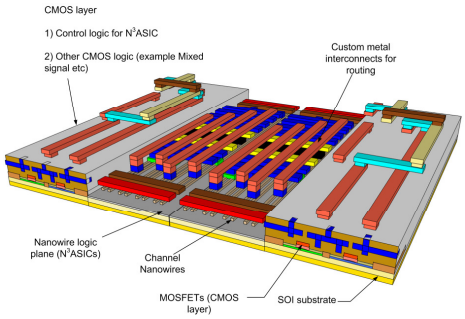

Fig. 2 A nano-CMOS 3D integrated fabric

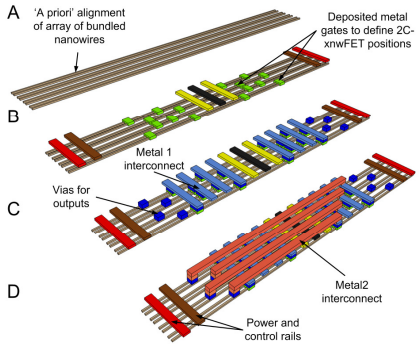

Fig. 3 A simplified manufacturing sequence

overlay requirements are removed ensuring finer nanoscale resolution (and consequently higher density) than can be achieved with lithography at the bottom.

In order to successfully achieve 3-D integration with good overlay precision, conventional lithography is used and CMOS design rules (Fig. 1) are followed for all subsequent steps such as creation of metal vias, interconnect, contact rails etc. Fig. 1 also shows the design rules across nanoscale features and lithographic scale length λ, to accommodate via placement. Pitch and spacing dimensions of the bottom nanowire grid must adhere to CMOS design rules.

A fabric incorporating these principles of 3-D integration is Nanoscale 3-D Application Specific Integrated Circuits (N^3ASICs)[9] (Fig. 2). The step-by-step 3-D integration approach for N^3ASICs is shown in Fig. 3. Nanowires may be direct-patterned on Silicon-on-Insulator substrates (Fig. 3A) through unconventional approaches such as SNAP and imprint lithography. Since metal vias are used as contacts for the channel nanowires, the spacing of the channel nanowires is determined by via spacing. Since channel nanowires could have much smaller dimensions than metal vias, they are bundled into pairs to make better contact, and provide for dual channel crossed-nanowire field-effect transistors (2C-xnwFETs) [9].

Following the *a priori* patterning of nanowire layers, masks are used for metal gate deposition. This step defines the positions of the transistors on the grid to achieve the required functionality (Fig. 3B). Finally, metal stacks implement interconnects as in traditional CMOS (Fig. 3C, 3D). The fabric can be built on a single SOI wafer, with nanowire logic plane surrounded by CMOS circuitry and is found to be 6X denser than CMOS.

III. Overlay Simulation Results

The WISP-0 nanoscale processor design [4] was mapped onto the N^3ASIC fabric mentioned above. Overlay misalignments were modelled as Gaussian random variables, and Monte Carlo simulations were carried out in a detailed logic simulator to determine the number of functioning chips. The simulations were carried for the 3σ overlay values projected by ITRS. The results in Fig. 4 show that close to 99% yield may be obtained for 3σ=±9nm overlay (manufacturable as per ITRS) when constructing a uniform nanowire bundle with λ=8nm (16nm technology node) in the 3D integrated fabric. Within a bundle widths of nanowires were 5nm, with 6nm spacing to accommodate 16nm vias. Fig. 4 shows that a pessimistic mask overlay with 3σ=±16nm results in a yield of 83%.

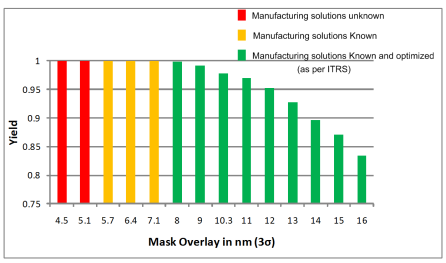

Fig. 4 Yield vs. Overlay for 3D integrated fabric

IV. Conclusion

We show that the design choices and the order of process aid in mitigating the impact of mask overlay. The proposed N^3ASIC fabric defined by a dense nanowire array at the bottom, followed by CMOS interconnect layers on the top is 6X denser than CMOS and is realizable with the available manufacturing techniques at very minimal yield loss. Any overlay precision better than 9nm results in a yield of 100%. In contrast, irregular structures would have more stringent mask overlay requirements.

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