

Yield and Routing Objectives in Floorplanning *

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Abstract

Traditionally the floorplan of a chip has been determined so as to minimize the total chip area and reduce the routing costs. Recently, it has been shown that the floorplan also affects the yield of the chip. Consequently, it becomes desirable to consider the expected yield, in addition to the cost of routing, when selecting a floorplan.

The goal of this paper is to study the two seemingly disjoint objectives of yield enhancement and routing complexity minimization, and find out whether they lead to different optimal floorplans, resulting in a need for a tradeoff analysis.

1. Introduction

Floorplanning is the partitioning of the entire chip area into smaller rectangles which will be occupied by the various given building blocks. In the case of a microprocessor, these building blocks (also called *modules*) are instruction cache, data cache, instruction decode unit, integer arithmetic and logic unit, and alike. When deciding on a floorplan, we take into account the preferred mutual position of the modules, which is determined by the number of nets that connect them. Two modules which have a large number of common nets should be placed as close as possible in order to reduce the total wiring length and obtain a high performance design by reducing the communication delays among the modules. Since at the floorplanning phase the complete routing has not yet been attempted, only rough estimates of the wiring length can be taken into account. A commonly used estimator for the wiring length of a given net is the rectilinear (Manhattan) distance between the centers of the two modules which are connected by the given net. Thus, the metric for the wiring length between two modules i and j which have M_{ij} nets in common, is given by

$$M_{ij} \cdot (|x_i - x_j| + |y_i - y_j|)$$

where (x_i, y_i) and (x_j, y_j) are the coordinates of the centers of i and j , respectively. The problem of finding the floorplan with the minimal wiring is, in the general case,

* This work was supported in part by JPL, under contract 961294, and by NSF, under contract MIP-9710130.

NP-complete. Various heuristic algorithms for solving it have been proposed and are currently being used [4, 9, 10, 11].

Until recently, VLSI designers rarely considered yield issues when selecting a floorplan for a newly designed chip. This is still justified for chips which are small and whose defect distribution can be accurately described by either the Poisson or the Compound Poisson yield models with large area clustering (i.e., the size of the defect clusters is larger than the size of the chip). For those chips, selecting a different floorplan will not affect the projected yield of the designed chip.

This situation is now changing with the introduction of integrated circuits with a total area of $2cm^2$ and up. These chips usually consist of different types of components with different device densities, and may have some incorporated redundancy. It has been shown in [5, 7] that if chips with these attributes are hit by medium sized defect clusters, then changes in the floorplan can affect their projected yield. It has been further shown that the optimal floorplan, from the yield point of view, depends on the defect densities of the modules. Since there is no direct relationship between the defect density of a module and its connectivity to the other modules, it is very likely that the floorplans with the smallest wiring cost will not have the highest possible yield. Clearly, minimizing the total wiring length, which impacts the performance of the chip, will always be more important than increasing the expected yield. There is a need, however, to study the two objectives (total wiring cost and yield) and explore the possibility of optimizing the yield with the minimum wiring cost as a constraint. Also, some trade-off between the two may be considered.

2. Problem Description

Multi-objective optimization problems in which two or more conflicting criteria appear simultaneously, occur frequently in engineering, economics, management, manufacturing, etc. [2, 3]. There is no clear cut solution to a multi-objective problem, since improving one objective will usually have a negative impact on the others. The two most frequently used approaches to attacking such a problem are weighting and Pareto optimization. In the first approach, a weight is attached to each objective according to its importance, and the weighted sum of the objectives is calculated for each solution point. The solution with the highest weighted sum is then selected. This approach changes the decision problem from multi-dimensional to one-dimensional. The second approach keeps the multi-dimensionality of the problem. Rather than selecting one solution, a set of "Pareto-optimal" solutions is found, so that none of the solutions in the set "dominates" any of the others, and all are considered equally good and equally "optimal". We will demonstrate these two approaches while solving the problem discussed in this paper.

Denoting the wiring cost by W and the yield by Y , the multi-objective is minimizing W and maximizing Y . These are usually conflicting objectives and cannot be accomplished simultaneously (except for some very special cases). In the weighting method, weights c_w and c_y are selected, and the optimal solution $s^* = (w^*, y^*)$ is the one which minimizes the function $Z = c_w W - c_y Y$.

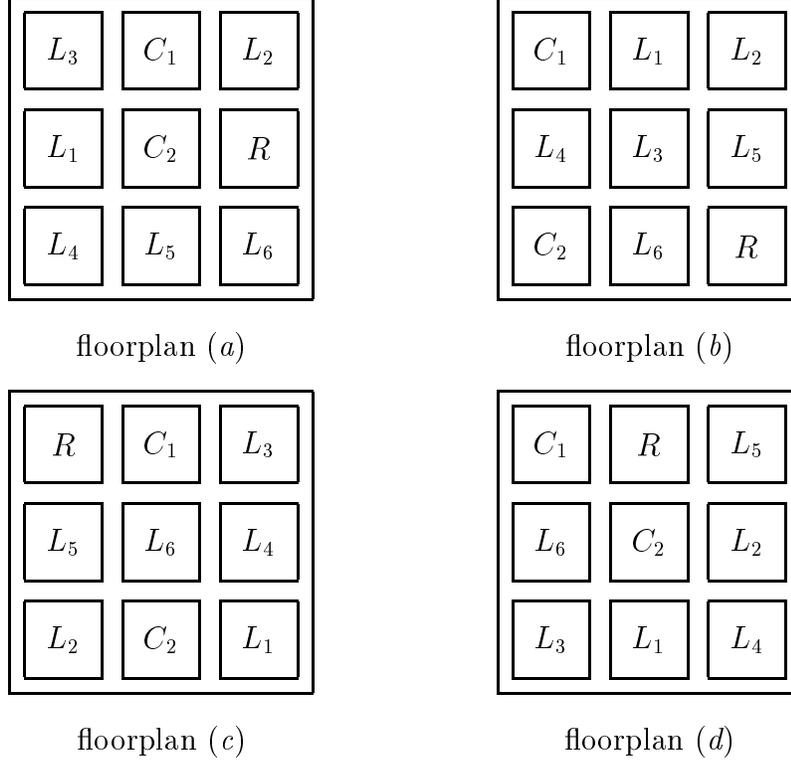


Figure 1. Four floorplans of a chip with nine modules.

To construct the "Pareto-optimal" set of solutions, we need the following definition:

Definition

Given two solutions, $s_1 = (w_1, y_1)$ and $s_2 = (w_2, y_2)$, we say that s_1 dominates s_2 , denoted by $s_1 \succ s_2$, if $w_1 \leq w_2$ and $y_1 \geq y_2$.

A set of solutions $\{s_1, \dots, s_n\}$ is called Pareto-optimal if no solution in the set dominates any other solution, i.e., for any s_i, s_j in the set, $s_i \not\succeq s_j$ and $s_j \not\succeq s_i$.

Specifically for our problem, a set of solutions is Pareto-optimal if for every s_i and s_j in the set (where $s_i = (w_i, y_i)$ and $s_j = (w_j, y_j)$), either $w_i < w_j$ and $y_i < y_j$, or $w_i > w_j$ and $y_i > y_j$, i.e., each solution is better in one aspect but worse in the other.

We next illustrate these two approaches through two examples.

3. Example I

In this example we examine a simple chip consisting of nine modules, all of the same size (see Figure 1). These nine units are a ROM (R), two static memory units (C_1 and C_2) (e.g., instruction cache and data cache), and six random logic units with different transistor densities (L_1, L_2, L_3, L_4, L_5 and L_6).

We assume that the defect densities of the different modules are proportional to the number of transistors per module. We also assume that the number of interconnects per module, N , follows Rent's rule [1], i.e.,

$$N = K_p \cdot g^\beta$$

where g is the number of gates in the module, and K_p and β are constants whose values depend on the type of the module. For example, for static memories $K_p = 6$ and $\beta = 0.12$, while for microprocessor logic units $K_p = 0.45$ and $\beta = 0.82$ [1]. We thus selected defect densities satisfying

$$\begin{aligned} & \lambda_R : \lambda_{C_1} : \lambda_{C_2} : \lambda_{L_1} : \lambda_{L_2} : \lambda_{L_3} : \lambda_{L_4} : \lambda_{L_5} : \lambda_{L_6} \\ & = 0.24 : 0.30 : 0.36 : 0.06 : 0.09 : 0.06 : 0.03 : 0.06 : 0.03 \end{aligned}$$

Denoting the vector $(R, C_1, C_2, L_1, \dots, L_6)$ by $(1, 2, \dots, 9)$, M_{ij} is the number of wires connecting modules i and j , $i, j = 1, \dots, 9$. We selected the resulting matrix M as

$$M = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 24 & 0 \\ 0 & 0 & 0 & 0 & 0 & 20 & 0 & 0 & 20 \\ 0 & 0 & 0 & 30 & 30 & 0 & 0 & 30 & 30 \\ 0 & 0 & 30 & 0 & 0 & 0 & 15 & 0 & 0 \\ 0 & 0 & 30 & 0 & 0 & 0 & 15 & 0 & 0 \\ 0 & 20 & 0 & 0 & 0 & 0 & 15 & 0 & 0 \\ 0 & 0 & 0 & 15 & 15 & 15 & 0 & 15 & 10 \\ 24 & 0 & 30 & 0 & 0 & 0 & 15 & 0 & 0 \\ 0 & 20 & 30 & 0 & 0 & 0 & 10 & 0 & 0 \end{pmatrix}$$

In addition to the inter-module connections we have also considered the wires to the chip pins. The numbers used were $M_{2,out} = 24$ and $M_{7,out} = 32$. The total number of wires per module was chosen so as to satisfy Rent's rule, i.e.,

$$N_i = \sum_{j=1}^9 M_{ij} + M_{i,out}$$

A floorplan of this chip can be represented as a permutation (n_1, \dots, n_9) of $(1, 2, \dots, 9)$. The yield model used for the yield analysis of the various floorplans is the medium-size clustering negative binomial model presented in [6], with a block size (i.e., "average defect cluster size") of 2×2 modules, and a clustering parameter $\alpha = 0.25$. As the wiring cost for a given floorplan we used

$$W = \sum_{i=1}^9 \sum_{j=1}^9 M_{n_i n_j} D_{ij}$$

where D_{ij} is the Manhattan distance between modules i and j in the chip and

$$D = \begin{pmatrix} 0 & 1 & 2 & 1 & 2 & 3 & 2 & 3 & 4 \\ 1 & 0 & 1 & 2 & 1 & 2 & 3 & 2 & 3 \\ 2 & 1 & 0 & 3 & 2 & 1 & 4 & 3 & 2 \\ 1 & 2 & 3 & 0 & 1 & 2 & 1 & 2 & 3 \\ 2 & 1 & 2 & 1 & 0 & 1 & 2 & 1 & 2 \\ 3 & 2 & 1 & 2 & 1 & 0 & 3 & 2 & 1 \\ 2 & 3 & 4 & 1 & 2 & 3 & 0 & 1 & 2 \\ 3 & 2 & 3 & 2 & 1 & 2 & 1 & 0 & 1 \\ 4 & 3 & 2 & 3 & 2 & 1 & 2 & 1 & 0 \end{pmatrix}$$

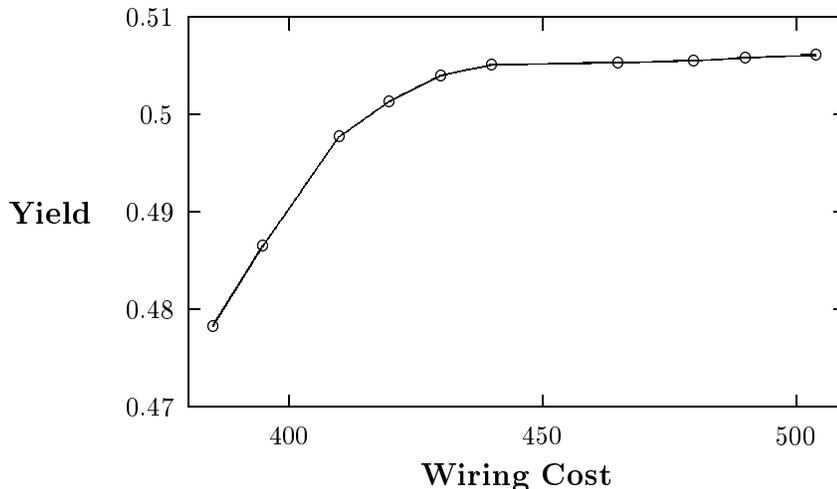


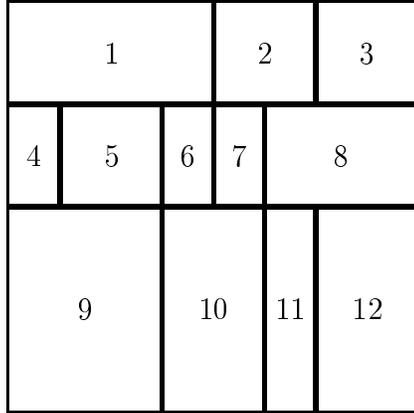
Figure 2. Optimal combinations of yield and wiring cost.

The floorplan with the highest overall yield (0.506) is shown in Figure 1(a). The floorplan with the lowest overall yield (0.458) is shown in Figure 1(b). The yield of the floorplan in Figure 1(a) is larger by 10% than that of the floorplan in Figure 1(b). Both these floorplans do not achieve the minimal wiring cost. Floorplans (a) and (b) have wiring costs of 504 and 650, respectively. Floorplan (c), shown in Figure 1(c), has the lowest wiring cost of 385 but a yield of only 0.478 (roughly half way between the highest and the lowest yields). Floorplan (d), shown in Figure 1(d), is an attempt to increase the yield with only a slight increase in the wiring cost. Its projected yield is 0.498 and its wiring cost is 410. In other words, for a 6.5% increase in wiring cost we can achieve a 4.1% increase in yield.

We next calculated the set of all Pareto-optimal floorplans, and they are depicted in Figure 2. Given appropriate weights c_w and c_y , one of these points can be selected so as to minimize $Z = c_w W - c_y Y$. Clearly, if $c_w \geq c_y$, then the first point, the one which minimizes the wiring length (and whose floorplan is shown in Figure 1(c)) will be chosen. If yield is of utmost importance, then the last point, in which the yield is the highest (and whose floorplan is shown in Figure 1(a)) will be selected. If, for example, $c_w = 1$ and $c_y = 1500$, then the floorplan in Figure 1(d) (represented in Figure 2 by the third point from the left) will be selected.

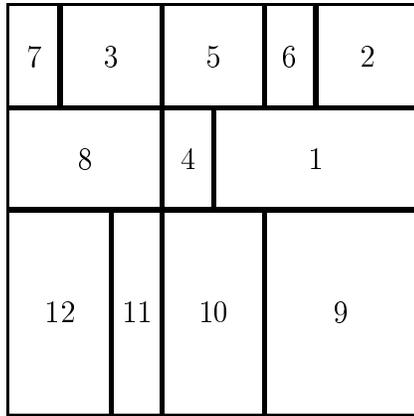
4. Example II

The second example is the floorplan of Matsushita's ADENART microprocessor [8]. This microprocessor has a 64-bit RISC superscalar architecture containing a data cache (DCU) and an instruction cache (ICU). It has been implemented in a $0.8\mu\text{m}$ CMOS technology and it contains 1300K transistors in a total area of $14.7 \times 15.3 \text{ mm}^2$. A simplified diagram of the chip's floorplan is depicted in Figure 3(a). The microprocessor includes two register files (FR – floating-point registers and PR – pointer registers), an instruction decode unit (IDU), a data bus control unit (DBC), a ROM and five execution units: a floating-point add and subtract unit (FAU), a

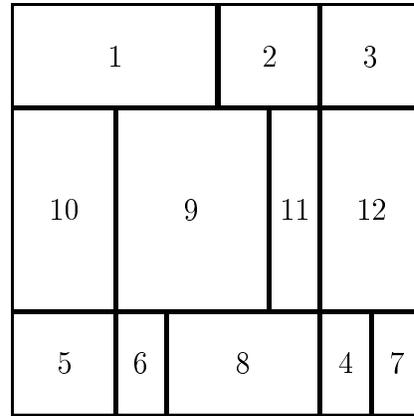


| Unit | Name | λ |
|------|------------|-------------------|
| 1 | <i>FCU</i> | λ_{lg-1} |
| 2 | <i>IDU</i> | λ_{lg-1} |
| 3 | <i>ICU</i> | λ_{cache} |
| 4 | <i>PR</i> | λ_{lg-4} |
| 5 | <i>PNU</i> | λ_{lg-2} |
| 6 | <i>LDU</i> | λ_{lg-2} |
| 7 | <i>ROM</i> | λ_{rom} |
| 8 | <i>FMU</i> | λ_{lg-3} |
| 9 | <i>DCU</i> | λ_{cache} |
| 10 | <i>DBC</i> | λ_{lg-5} |
| 11 | <i>FR</i> | λ_{lg-4} |
| 12 | <i>FAU</i> | λ_{lg-3} |

floorplan (a) – the original floorplan (simplified)



floorplan (b)



floorplan (c)

Figure 3. The original and two alternative floorplans for the ADENART chip.

floating-point multiply and divide unit (FMU), a load address add unit (LDU), a pointer arithmetic and logic unit (PNU) and a flow control unit (FCU). The twelve modules have six different transistor densities with the ROM having the highest density and the FCU and IDU, the lowest density. Assuming that the fault densities are linearly proportional to the transistor densities we define six fault densities which satisfy

$$\lambda_{lg-1} < \lambda_{lg-2} < \lambda_{lg-3} < \lambda_{lg-4} < \lambda_{lg-5} < \lambda_{cache} < \lambda_{rom}$$

These fault densities are assigned to the individual modules as shown in Figure 3(a). Based on the transistor densities reported in [8], the approximate fault densities satisfy

$$\begin{aligned} \lambda_{rom} : \lambda_{cache} : \lambda_{lg-5} : \lambda_{lg-4} : \lambda_{lg-3} : \lambda_{lg-2} : \lambda_{lg-1} \\ = 8.88 : 7.69 : 3.27 : 2.42 : 2.27 : 1.69 : 1 \end{aligned}$$

As an interconnect matrix, we used the matrix

$$M = \begin{pmatrix} 0 & 0 & 32 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 64 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 32 & 64 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 96 & 96 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 96 & 0 & 0 & 0 & 0 & 32 & 0 & 0 & 0 \\ 0 & 0 & 0 & 96 & 0 & 0 & 0 & 0 & 32 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 32 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 32 & 0 & 0 & 0 & 192 & 0 \\ 0 & 0 & 0 & 0 & 32 & 32 & 0 & 0 & 0 & 160 & 192 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 160 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 192 & 192 & 0 & 0 & 192 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 192 & 0 \end{pmatrix}$$

As the number of wires to the chip pins we used $M_{3,out} = 64$ and $M_{10,out} = 160$.

A floorplan of this chip can be represented by (n_1, \dots, n_{12}) , where n_1, \dots, n_{12} is a permutation of $1, \dots, 12$, although not all permutations can serve as floorplans due to the different sizes of the modules. As the yield model we again used the medium-size clustering negative binomial distribution, with a block size equal to a quarter of the chip, and a clustering parameter $\alpha = 0.25$. We calculated all the Pareto-optimal points with regards to wiring length and yield, and they are depicted in Figure 4. The floorplans with the highest and lowest yield are depicted in Figure 3(b) and 3(c),

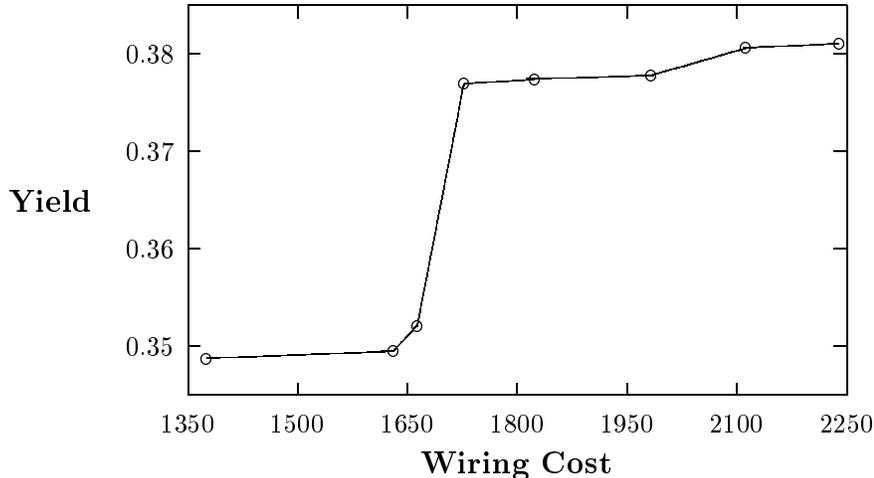


Figure 4. Optimal combinations of yield and wiring cost.

respectively. In addition, we calculated the yield distribution among all floorplans and among the floorplans with the lowest wiring costs, and these are shown in Figure 5. We can conclude from Figure 5 that if the selection of the floorplan is based solely on wiring costs, it is more likely to result in a lower yield than a higher yield. Similarly, Figure 6 depicts the distribution of the wiring length of all floorplans, and that of the floorplans with the highest yields. Unlike Figure 5, the two distributions in Figure 6 are almost similar leading to the conclusion that restricting to floorplans

with high yield will not greatly impact the selection of a floorplan with a low wiring cost.

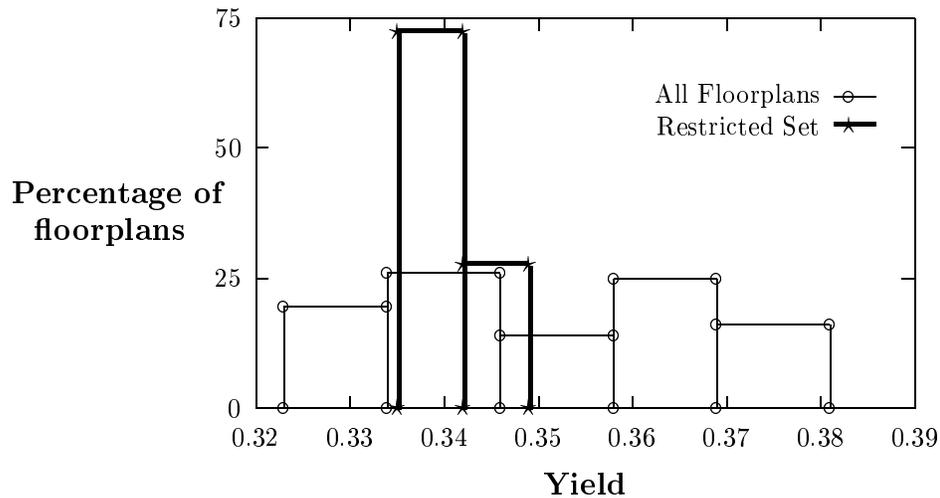


Figure 5. The distribution of yield for all floorplans and for low wiring cost floorplans.

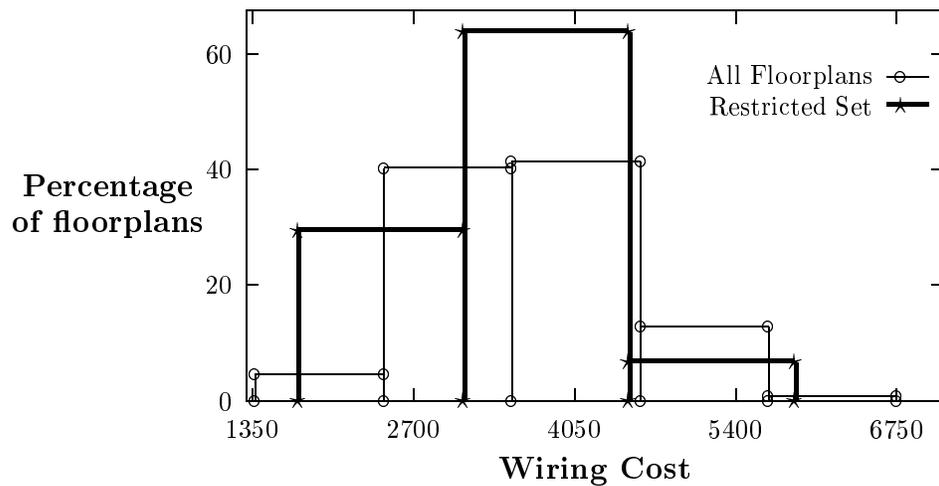


Figure 6. The distribution of wiring cost for all floorplans and for high yield floorplans.

5. Conclusions

We have studied in this paper two distinct objectives in floorplanning, namely, total wiring length minimization and yield maximization. Since these objectives are often conflicting, a set of Pareto-optimal solutions is introduced, and one of these solutions is selected according to the relative importance of each of the two objectives. We

showed that even if the wiring length is considered of utmost importance, the yield can still be maximized within the set of floorplans with the minimal wiring length or very close to it.

References

- [1] H.B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI*, Addison-Wesley, Reading, Massachusetts, 1990.
- [2] V. Chankong and Y. Y. Haimes, *Multiobjective Decision Making: Theory and Methodology*, North-Holland, New York NY, 1983.
- [3] G. Evans, "Overview of Techniques for Solving Multiobjective Mathematical Programs," *Management Science*, Vol. 30, No. 11, pp 1268-1282, November 1984.
- [4] T. Lengauer, *Combinatorial Algorithms for Integrated Circuit Layout*, John Wiley & Sons, West Essex, England, 1990.
- [5] Z. Koren and I. Koren, "Does the Floorplan of a Chip Affect Its Yield?" *Proc. of the 1993 IEEE Internl. Workshop on Defect and Fault Tolerance in VLSI Systems*, pp. 159-166, October 1993.
- [6] I. Koren, Z. Koren and C.H. Stapper, "A Unified Negative Binomial Distribution for Yield Analysis of Defect Tolerant Circuits," *IEEE Trans. on Computers*, Vol. 42, pp. 724-437, June 1993.
- [7] Z. Koren and I. Koren, "On the Effect of Floorplanning on the Yield of Large Area Integrated Circuits," *IEEE Trans. on VLSI Systems*, Vol. 5, pp. 3-14, March 1997.
- [8] H. Nakano, M. Nakajima, Y. Nakakura and T. Yoshida, "An 80-MFLOPs (Peak) 64-b Microprocessor for Parallel Computer," *IEEE Journal of Solid-State Circuits*, vol. 27, pp. 365-371, March 1992.
- [9] S. Wimer and I. Koren, "Analysis of Strategies for Constructive General Block Placement," *IEEE Trans. on Computer-Aided Design*, Vol. 7, pp. 371-377, March 1988.
- [10] S. Wimer, I. Koren and I. Cederbaum, "Optimal Aspect Ratios of Building Blocks in VLSI," *IEEE Trans. on Computer-Aided Design*, Vol. 8, pp. 139-145, Feb. 1989.
- [11] S. Wimer, I. Koren and I. Cederbaum, "Optimal Determination of Block Dimensions in General Floorplans," *Routing, Placement and Partitioning*, G.W. Zobrist (ed.), Ch. 7, pp. 237-286, Ablex Publishing Corp., 1994.