Techniques for Yield Enhancement of VLSI Adders [1]

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Abstract

For VLSI application-specific arrays and other regular VLSI circuits, two techniques are available for yield enhancement, namely defect-tolerance and layout modifications. In this paper, we compare these two yield enhancement approaches by using adders as an example. Our yield projections indicate that the layout modification technique is more efficient when the defect density is low, while reconfiguration is more efficient for a high defect density. However, from the point of the view of effective yield, the layout modification is superior to defect tolerance in the practical range of defect density.

1 Introduction

Numerous techniques for incorporating redundancy into regular VLSI arrays in order to increase their manufacturing yield have been proposed[1]. Most of these techniques attempt to minimize the area overhead by taking advantage of the regular structure of such arrays. Another approach for yield enhancement of VLSI circuits is based on layout modification techniques which attempt to minimize the sensitivity of the layouts to fabrication defects (e.g.,[2]). Such techniques usually incur no (or very small) area overhead. For VLSI circuits with no regular structure, the layout modification approach is the only choice for yield enhancement. However, for regular VLSI arrays, yield enhancement can also be achieved through defect tolerance techniques.

The objective of this paper is to compare these two alternative approaches for yield enhancement of regular VLSI designs using VLSI adders as an example. In Section 2 and Section 3, we apply these two yield enhancement methods to several types of adder designs to improve their yield. The comparison of the two methods and some conclusions are presented in Section 4 and Section 5, respectively.

2 Yield enhancement through reconfiguration

Following the circuit structure and reconfiguration scheme proposed in [3]-[5], several 16-bit defect-tolerant adders with a single spare bit slice have been designed using 2-micron CMOS technology. In our design, a bit-slice structure was chosen to make the adders more regular and thus suitable for reconfiguration. Besides the 16 single-bit slices, one spare slice is provided to replace the defective one. The use of laser fuses to disconnect the defective elements and connect the good ones is assumed. The area, delay, area overhead, and reconfigurability of the designed adders are shown in Table 1. The reconfigurability measure is defined as the percentage of chip area that is reconfigurable, i.e., the area in which faults can be tolerated.

Not all types of adders are suitable for this kind of structure. For example, a *carry-look-ahead* adder has a non-regular structure, and the required hardware overhead for defect-tolerance is prohibitively high, so it is not a good candidate for hardware redundancy.

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Type of adder	Area (10^5 μm^2)	Delay (ns)	Overhead(%)	Reconfigurability(%)
ripple-carry	2.65	28.3	34	74
Manchester	2.44	14.7	35	71
carry-skip	3.46	11.3	27	57
carry-select	5.97	9.2	30	65
conditional-sum	6.07	10.6	31	62

Table 1: Area, speed, hardware overhead and reconfigurability of different adders.

In addition to the three types of adders reported in [3]-[5], i.e., *ripple-carry, Manchester*, and *carry-skip*, we found that *carry-select* and *conditional-sum* [6] are also good candidates when the criteria of area overhead and percentage of reconfigurable circuitry are considered. Figure 1 shows the design of a defect-tolerant *carry-select* adder and the reconfiguration of signals propagated between slices when a fault occurs. Other adders have similar reconfiguration schemes.

The main purpose of incorporating redundancy into the design of adders is yield enhancement. In order to calculate the yield, we used the negative binomial yield model under the large area clustering assumption, with an average of λ faults per unit area and a clustering parameter of α. Under this model, the yield of an adder without redundancy is [7]:

$$Y = Y_0(1 + \lambda A_c/\alpha)^{\alpha} \tag{1}$$

where Y_0 is the gross yield factor and A_c is the critical area.

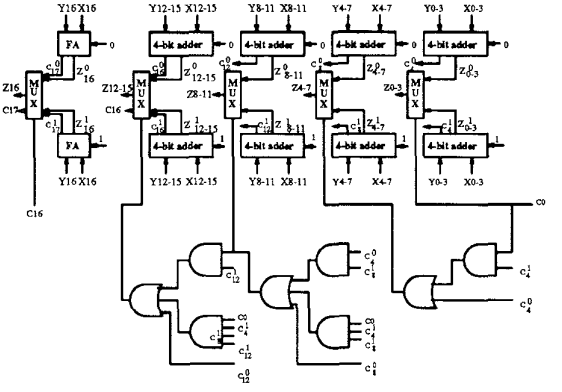
For a 16-bit adder with one spare slice, the yield estimation is slightly more complex. Here, we need to distinguish between the reconfigurable part and the nonreconfigurable part. The nonreconfigurable part includes power and ground lines, switching circuitry, etc. Each fault occurring in the nonreconfigurable part can cause a chip-kill fault[7]. Let A_{ck} denote the critical area of the nonreconfigurable circuit, and A_{cm} denote the critical area of a standard one bit module. Then the yield of the defect-tolerant adder is [7][8]:

$$Y = Y_0 \sum_{M=16}^{17} a_{M,17} \tag{2}$$

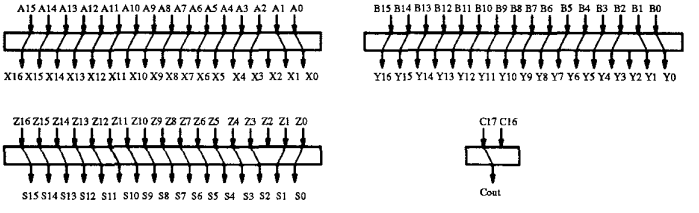
where

$$\begin{aligned} a_{M,N} &= Prob[Exactly\ M\ out\ of\ the\ N\ modules\ are\ fault\ free] \\ &= \sum_{K=0}^{N-M} (-1)^K \begin{pmatrix} N-M \\ K \end{pmatrix} \begin{pmatrix} N \\ M \end{pmatrix} \left(1 + \frac{\lambda A_{ck} + \lambda A_{cm}(M+K)}{\alpha}\right)^{-\alpha} \end{aligned}$$

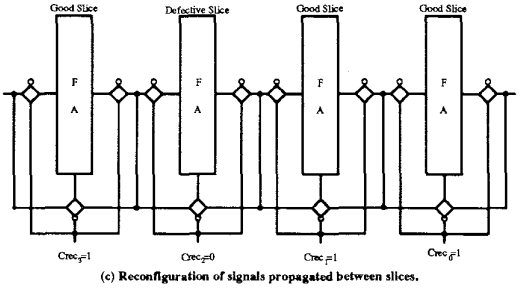
In all the following yield calculations, we consider only six types of defects, which are *metal1 open, metal1 short, poly open, poly short, metal2 open*, and *metal2 short*. The yield analysis tool XLASER [9] is used to estimate the critical area for each type of defects. To



(a) 16-bit carry-slelect adder with one spare bit slice



(b) Switching circuit when bit 2 is defective.



(c) Reconfiguration of signals propagated between slices.

Figure 1: Design of a defect-tolerant *carry-select* adder.

simplify the calculation, we also assume that all the three short-circuit type defects have the same density and that it is 10 times as high as the density for the three open-circuit type defects[10], which are also assumed to have the same density. We further assume a clustering parameter $\alpha = 1$ and a gross yield factor $Y_0 = 98\%$.

Using formulas (1) and (2), we can calculate the yield of the five types of adders under different defect densities. Figure 2 shows the yield projection results of three out of the five adders.

As expected, *ripple-carry* has a relatively high yield, mainly due to its small chip area. We also find, as one might expect, that the role of redundancy becomes more important to yield enhancement as the defect density increases.

3 Yield enhancement through layout modifications

Layout modification is another technique that can be used to achieve yield enhancement [2][11], this is because wider lines can reduce the layout sensitivity to open-circuit type faults, and larger spacing between conducting lines can reduce layout sensitivity to short-circuit type faults. To study this approach, layouts of three types of adders (*ripple-carry, carry-skip*, and *carry-select*) have been modified to make them less sensitive to defects. The rules of layout modifications we have used in the design of the three adders are:

1. Keep overall circuit structure unchanged;
2. Do not change the layouts of the active region;
3. Only conducting lines in the poly, metal1 and metal2 layers should be modified.
4. Layouts after modifications should occupy almost the same area as the layouts of adders that incorporate redundancy, to allow a more meaningful comparison of the results of these two yield enhancement techniques.

Using formulas (1) and (2), we compute the yields of the three types of adders, and the results are shown in Figure 3. Figure 4 shows the layouts of a full-adder before and after layout modifications.

4 Comparison of the two yield enhancement approaches

In Table 2, the yield improvement rates for three different adders using the two yield enhancement techniques have been listed. From this table, we find that in most cases, adders with hardware redundancy have a better yield than adders with modified layouts, except for *carry-skip* when $\lambda = 1\ cm^{-2}$. Does this mean that hardware redundancy is more efficient than layout modifications? A further study shows that, when defect density drops below 1 cm^{-2}, adders with modified layouts may have a higher yield. Figure 5 shows the yield of *ripple-carry* (RC) and *carry-select* (CS) as a function of defect density, in which yield curves change their relative positions and cross each other for both of the adders. This shows that layout modifications (LM) are more suitable when defect density is low, while circuit reconfiguration (CR) is more effective when defect density is high.

In practice, the effective yield, which reflects the expected number of good chips on a given wafer area, is a more important measure. However, due to the small area of 16-bit adders and their high yield, any attempt to improve yield at the cost of chip area cannot be justified, if 16-bit adders are fabricated as separate chips. This does not mean that yield

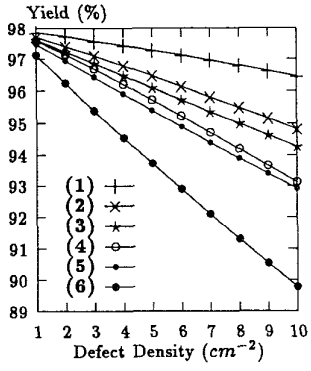
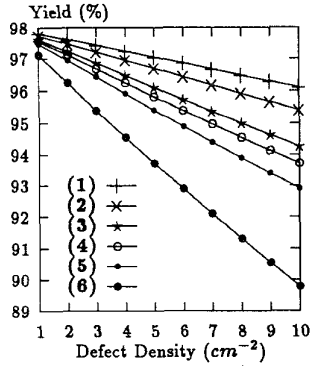
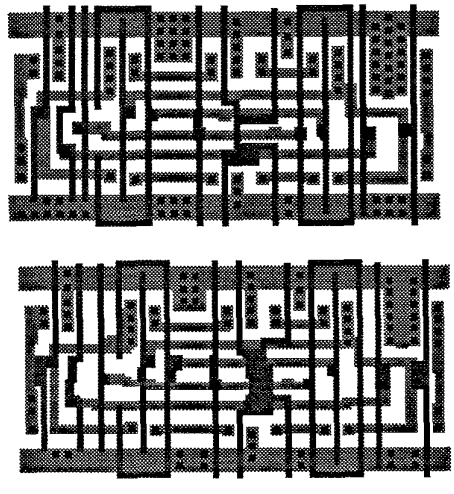


Figure 2: Yield of adders with and without redundancy.



(1) *ripple-carry(w/)* (3) *ripple-carry(w/o)* (5) *carry-skip(w/o)*
(2) *carry-skip(w/)* (4) *carry-select(w/)* (6) *carry-select(w/o)*

Figure 3: Yield of adders with and without layout modification.



(a) Original layout.

(b) Modified layout.

Figure 4: Layout of a full-adder with and without layout modifications.

Type of Adders	Yield Improvement Rate of Adders					
	λ=1 cm^{-2}		λ=5 cm^{-2}		λ=10 cm^{-2}	
	Reconfi-guration	Layout Modification	Reconfi-guration	Layout Modification	Reconfi-guration	Layout Modification
ripple-carry	0.26	0.20	1.3	0.99	2.5	1.9
carry-skip	0.25	0.27	1.3	1.3	2.6	2.4
carry-select	0.49	0.43	2.4	2.2	4.7	4.4

Table 2: Yield improvement rate after introducing different yield enhancement techniques.

enhancement for adders is not needed. In most cases, adders constitute only a small part of microprocessors or other VLSI circuits and consequently, the ratio of adder area increase to the whole chip area is very small; sometimes there is no increase at all. As a result, increasing the adder area can still improve the effective yield of the whole chip.

One of the methods commonly used in the yield study of a small portion of a VLSI circuit is to duplicate the small circuit to make a large chip. We can apply this method in the comparison of the effective yield of adders with different yield enhancement approaches. Though the adder arrays introduced here do not have much practical meaning, the results we get from the adder arrays can be applied to a wide-range of VLSI circuits for the following reasons:

1. Many application-specific VLSI chips have an array of arithmetic units. We can apply our results of adder arrays to these chips if, in each arithmetic unit, we use similar yield enhancement techniques as in the adders and get a similar yield improvement rate.
2. Even for a VLSI chip with no array structure, we can still divide the whole circuit into different subcells. The yield behavior of the chip will be similar to the adder array if, in each subcell, we use similar yield enhancement techniques as in the adders and obtain a similar yield improvement rate.

We consider five versions of a 20 × 20 *ripple-carry* adder array:

- **Version 1:** Original version, without taking yield into consideration;
- **Version 2:** Layout modification version with the same area as **Version 1**;
- **Version 3:** Hardware redundancy version, as was done in Section 2;
- **Version 4:** Layout modification version with almost the same area as **Version 3**, as was done in Section 3;
- **Version 5:** Another layout modification version, with a smaller area overhead (about 5%).

The effective yield is calculated using the following formula:

$$Y_{effective\_i} = Y_i \cdot \frac{Area_{version\_i}}{Area_{version\_1}} \tag{3}$$

where Y_i is the yield of version i. The effective yield improvement rate for versions 2, 3, 4 and 5 is shown in Figure 6.

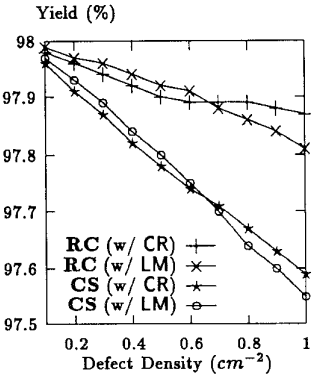


Figure 5: Yield as a function of defect density.

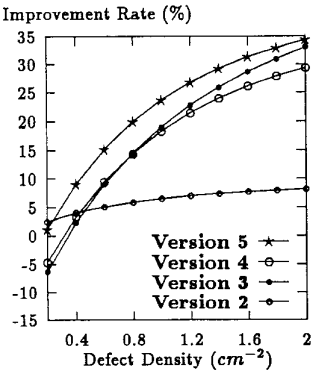


Figure 6: Effective yield improvement rate as a function of defect density.

From Figure 6, we find that when the defect density is low (less than $0.25cm^{-2}$), **Version 2**, the layout modification version with no extra area, has the highest effective yield; when the defect density is higher than $0.25cm^{-2}$, **Version 5**, the layout modification version with a small area overhead, has the highest yield. We also find that in order to get a optimal effective yield, only a small extra area is needed in the layout modification approach. Too much extra area will have a negative effect on the effective yield, and this is illustrated in Figure 6 by the fact that **Version 4** has a lower effective yield than **Version 5**. It is worthwhile to notice that layout modification (**Version 5**) is superior to defect tolerance (**Version 3**) when the defect density is less than $2cm^{-2}$, which means that in the practical range of defect density, we can get a higher effective yield if we adopt layout modification other than defect tolerance as our yield enhancement technique.

5 Conclusions

In this paper, we have studied two yield enhancement approaches used in the design of regular VLSI circuits. Our results show that, in a low defect density environment, the approach of layout modification is superior to circuit reconfiguration. However, when the defect density is high, the approach of reconfiguration seems to be a better choice. We have also compared the effective yield of adders with different yield enhancement techniques, and the results indicate that when defect density is less than $2cm^2$, the layout modification version is better than the defect tolerance version. As the defect density keeps decreasing as a result of the improvement in manufacturing facilities, the layout modification approach will prove to be a more important yield enhancement technique in the future. Though these conclusions are based on a study of adders, we expect them to hold for many other regular VLSI circuits as well.

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