HW Dynamic Scheduling

- Enables out-of-order execution and allows out-of-order completion
- All instructions pass through issue stage in order (in-order issue)
- Split the ID pipe stage of pipeline into 2 stages:
  - Issue—Decode instructions, check for structural hazards
  - Read operands—Wait until no data hazards, then read operands
Dynamic Scheduling: Tomasulo's Algorithm

♦ For IBM 360/91
♦ Goal: High Performance without special compilers
♦ Small number of floating point registers (4 in 360) prevented interesting compiler scheduling of operations
  • This led Tomasulo to try to figure out how to get more effective registers — renaming in hardware!
♦ Why Study 1966 Computer?
♦ The descendants of this have flourished!
  • Alpha 21264, HP 8000, MIPS 10000, Pentium, PowerPC, ...

Tomasulo Algorithm

♦ Control & buffers distributed with Functional Units (FU)
  • FU buffers called ”reservation stations”; have pending operands
♦ Registers in instructions replaced by values or pointers to reservation stations (RS):
  • form of register renaming;
  • avoids WAR, WAW hazards
  • More reservation stations than registers, so can do optimizations compilers can’t
♦ Results to FU from RS, not through registers, over Common Data Bus that broadcasts results to all FUs
♦ Load and Stores treated as FUs with RSs as well
Tomasulo’s Organization

Common Data Bus (CDB)

Reservation Station Components

**Op:** Operation to perform in the unit (e.g., ADD)

**Vj, Vk:** Value of Source operands

- Store buffers has Vj field, result to be stored

**Qj, Qk:** Reservation stations producing source registers (value to be written)

- Note: Qj, Qk=0 => ready

**Busy:** Indicates reservation station or FU is busy

**Register result status** — Indicates which functional unit will write each register, if one exists.
Blank when no pending instructions that will write that register.
Three Phases of Tomasulo’s Algorithm

1. Issue—get instruction from FP Op Queue
   If reservation station free (no structural hazard),
   control issues instruction & gets operands (renames registers)

2. Execute—operate on operands (EX)
   When both operands ready then execute;
   if not ready, watch Common Data Bus for result

3. Write result—finish execution (WB)
   Write on Common Data Bus to all awaiting units;
   mark reservation station available

   ♦ Normal data bus: data + destination (“go to” bus)
   ♦ Common data bus: data + source (“come from” bus)
     - 64 bits of data + 4 bits of Functional Unit (RS) source address
     - Does the broadcast
     - Other RS get data if matches expected Functional_Unit/RS
       (producing result)

   ♦ Example - speed of operations:
     2 clocks for Fl.pt.ADD_SUB and LOAD;  
     10 for MULT;        40 clocks for DIV

Tomasulo Example

Instruction stream

Instruction status:

<table>
<thead>
<tr>
<th>Instruction</th>
<th>j</th>
<th>k</th>
<th>Issue</th>
<th>Comp</th>
<th>Result</th>
<th>Busy</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD</td>
<td>F6</td>
<td>34+</td>
<td>R2</td>
<td></td>
<td></td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>LD</td>
<td>F2</td>
<td>45+</td>
<td>R3</td>
<td></td>
<td></td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>MULTD</td>
<td>F0</td>
<td>F2</td>
<td>F4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SUBD</td>
<td>F8</td>
<td>F6</td>
<td>F2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DIVD</td>
<td>F10</td>
<td>F6</td>
<td>F8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADDD</td>
<td>F6</td>
<td>F8</td>
<td>F2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Reservation Stations:

<table>
<thead>
<tr>
<th>Name</th>
<th>S1</th>
<th>S2</th>
<th>RS</th>
<th>RS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add1</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Add2</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Add3</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mult1</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mult2</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Register result status:

Clock cycle counter

<table>
<thead>
<tr>
<th>Clock</th>
<th>FU</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>F0 F2 F4 F6 F8 F10 F12 ... F30</td>
</tr>
</tbody>
</table>

3 Load/Buffers
3 FP Adder R.S.
2 FP Mult R.S.
Tomasulo Example Cycle 1

**Instruction status:**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>j</th>
<th>k</th>
<th>Issue</th>
<th>Comp</th>
<th>Result</th>
<th>Busy</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD</td>
<td>F6</td>
<td>34+</td>
<td>R2</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>LD</td>
<td>F2</td>
<td>45+</td>
<td>R3</td>
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<td></td>
<td></td>
<td>2</td>
</tr>
<tr>
<td>MULTD</td>
<td>F0</td>
<td>F2</td>
<td>F4</td>
<td></td>
<td></td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>SUBD</td>
<td>F8</td>
<td>F6</td>
<td>F2</td>
<td></td>
<td></td>
<td></td>
<td>4</td>
</tr>
<tr>
<td>DIVD</td>
<td>F10</td>
<td>F9</td>
<td>F6</td>
<td></td>
<td></td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>ADDD</td>
<td>F6</td>
<td>F8</td>
<td>F2</td>
<td></td>
<td></td>
<td></td>
<td>6</td>
</tr>
</tbody>
</table>

**Reservation Stations:**

<table>
<thead>
<tr>
<th>Time</th>
<th>Name</th>
<th>Busy</th>
<th>Op</th>
<th>Vj</th>
<th>Vk</th>
<th>Qj</th>
<th>Qk</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Add1</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Add2</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Add3</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Mult1</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Mult2</td>
<td>No</td>
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</tbody>
</table>

**Register result status:**

<table>
<thead>
<tr>
<th>Clock</th>
<th>F0</th>
<th>F2</th>
<th>F4</th>
<th>F6</th>
<th>F8</th>
<th>F10</th>
<th>F12</th>
<th>...</th>
<th>F30</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>FU</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Busy Address:**

- Load1 Yes 34+R2
- Load2 Yes 45+R3
- Load3 No

**Note:** Can have multiple loads outstanding

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Tomasulo Example Cycle 2

**Instruction status:**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>j</th>
<th>k</th>
<th>Issue</th>
<th>Comp</th>
<th>Result</th>
<th>Busy</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD</td>
<td>F6</td>
<td>34+</td>
<td>R2</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>LD</td>
<td>F2</td>
<td>45+</td>
<td>R3</td>
<td></td>
<td></td>
<td></td>
<td>2</td>
</tr>
<tr>
<td>MULTD</td>
<td>F0</td>
<td>F2</td>
<td>F4</td>
<td></td>
<td></td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>SUBD</td>
<td>F8</td>
<td>F6</td>
<td>F2</td>
<td></td>
<td></td>
<td></td>
<td>4</td>
</tr>
<tr>
<td>DIVD</td>
<td>F10</td>
<td>F9</td>
<td>F6</td>
<td></td>
<td></td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>ADDD</td>
<td>F6</td>
<td>F8</td>
<td>F2</td>
<td></td>
<td></td>
<td></td>
<td>6</td>
</tr>
</tbody>
</table>

**Reservation Stations:**

<table>
<thead>
<tr>
<th>Time</th>
<th>Name</th>
<th>Busy</th>
<th>Op</th>
<th>Vj</th>
<th>Vk</th>
<th>Qj</th>
<th>Qk</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Add1</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Add2</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Add3</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Mult1</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Mult2</td>
<td>No</td>
<td></td>
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<td></td>
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<td></td>
</tr>
</tbody>
</table>

**Register result status:**

<table>
<thead>
<tr>
<th>Clock</th>
<th>F0</th>
<th>F2</th>
<th>F4</th>
<th>F6</th>
<th>F8</th>
<th>F10</th>
<th>F12</th>
<th>...</th>
<th>F30</th>
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</thead>
<tbody>
<tr>
<td>2</td>
<td>FU</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Busy Address:**

- Load1 Yes 34+R2
- Load2 Yes 45+R3
- Load3 No

**Note:** Can have multiple loads outstanding
### Tomasulo Example Cycle 3

**Instruction status:**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Exec</th>
<th>Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD F6</td>
<td>34+</td>
<td>R2</td>
</tr>
<tr>
<td>LD F2</td>
<td>45+</td>
<td>R3</td>
</tr>
<tr>
<td>MULTD F0</td>
<td>F2</td>
<td>F4</td>
</tr>
<tr>
<td>SUBD F8</td>
<td>F6</td>
<td>F2</td>
</tr>
<tr>
<td>DIVD F10</td>
<td>F0</td>
<td>F6</td>
</tr>
<tr>
<td>ADDD F6</td>
<td>F8</td>
<td>F2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Instruction status</th>
<th>j</th>
<th>k</th>
<th>Issue</th>
<th>Comp</th>
<th>Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>Busy</td>
<td>Address</td>
<td>Name</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load1</td>
<td>Yes</td>
<td>34+R2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load2</td>
<td>Yes</td>
<td>45+R3</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Reservation Stations:**

<table>
<thead>
<tr>
<th>Time</th>
<th>Name</th>
<th>Busy</th>
<th>Op</th>
<th>Vj</th>
<th>Vk</th>
<th>Qj</th>
<th>Qk</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add1</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Add2</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Add3</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mult1</td>
<td>Yes</td>
<td>MULTD</td>
<td>R(F4)</td>
<td>Load2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mult2</td>
<td>No</td>
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</tr>
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</table>

**Register result status:**

<table>
<thead>
<tr>
<th>Clock</th>
<th>FU</th>
<th>Mult1</th>
<th>Load2</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Multi</td>
<td>Load2</td>
<td></td>
</tr>
</tbody>
</table>

- Note: MULT issued; registers names are removed ("renamed") in Reservation Stations
- Load1 completing; what is waiting for Load1?

---

### Tomasulo Example Cycle 4

**Instruction status:**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Exec</th>
<th>Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD F6</td>
<td>34+</td>
<td>R2</td>
</tr>
<tr>
<td>LD F2</td>
<td>45+</td>
<td>R3</td>
</tr>
<tr>
<td>MULTD F0</td>
<td>F2</td>
<td>F4</td>
</tr>
<tr>
<td>SUBD F8</td>
<td>F6</td>
<td>F2</td>
</tr>
<tr>
<td>DIVD F10</td>
<td>F0</td>
<td>F6</td>
</tr>
<tr>
<td>ADDD F6</td>
<td>F8</td>
<td>F2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Instruction status</th>
<th>j</th>
<th>k</th>
<th>Issue</th>
<th>Comp</th>
<th>Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>Busy</td>
<td>Address</td>
<td>Name</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load1</td>
<td>No</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load2</td>
<td>Yes</td>
<td>45+R3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load3</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Reservation Stations:**

<table>
<thead>
<tr>
<th>Time</th>
<th>Name</th>
<th>Busy</th>
<th>Op</th>
<th>Vj</th>
<th>Vk</th>
<th>Qj</th>
<th>Qk</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add1</td>
<td>Yes</td>
<td>SUBD</td>
<td>M(A1)</td>
<td>Load2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Add2</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Add3</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mult1</td>
<td>Yes</td>
<td>MULTD</td>
<td>R(F4)</td>
<td>Load2</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Mult2</td>
<td>No</td>
<td></td>
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</table>

**Register result status:**

<table>
<thead>
<tr>
<th>Clock</th>
<th>FU</th>
<th>Mult1</th>
<th>Load2</th>
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</thead>
<tbody>
<tr>
<td>4</td>
<td>Multi</td>
<td>Load2</td>
<td>0000</td>
</tr>
</tbody>
</table>

- Load2 completing; what is waiting for Load2?
Tomasulo Example Cycle 5

Instruction status:

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<tr>
<th>Instruction</th>
<th>j</th>
<th>k</th>
<th>Issue</th>
<th>Comp</th>
<th>Result</th>
<th>Busy</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD</td>
<td>F6</td>
<td>34+</td>
<td>R2</td>
<td>1</td>
<td>3</td>
<td>4</td>
<td>Load1</td>
</tr>
<tr>
<td>LD</td>
<td>F2</td>
<td>45+</td>
<td>R3</td>
<td>2</td>
<td>4</td>
<td>5</td>
<td>Load2</td>
</tr>
<tr>
<td>MULTD</td>
<td>F0</td>
<td>F2</td>
<td>F4</td>
<td></td>
<td></td>
<td>3</td>
<td>Load3</td>
</tr>
<tr>
<td>SUBD</td>
<td>F8</td>
<td>F6</td>
<td>F2</td>
<td>4</td>
<td></td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>DIVD</td>
<td>F10</td>
<td>F9</td>
<td>F6</td>
<td></td>
<td></td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>ADDD</td>
<td>F6</td>
<td>F8</td>
<td>F2</td>
<td></td>
<td></td>
<td>No</td>
<td></td>
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</table>

Reservation Stations:

<table>
<thead>
<tr>
<th>Time</th>
<th>Name</th>
<th>Busy</th>
<th>Op</th>
<th>Vj</th>
<th>Vk</th>
<th>Qj</th>
<th>Qk</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>Add1</td>
<td>Yes</td>
<td>SUBD</td>
<td>M(A1)</td>
<td>M(A2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
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<td>10</td>
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<td>Yes</td>
<td>MULTD</td>
<td>M(A2)</td>
<td>R(F4)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
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- Timer starts down for Add1, Mult1

Tomasulo Example Cycle 6

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- Issue ADDD here despite name dependency on F6?
Tomasulo Example Cycle 7

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• Add1 (SUBD) completing; what is waiting for it?

Tomasulo Example Cycle 8

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ECE68/Koren Part.6.15
Adapted from UCB and other sources
Copyright UCB & Morgan Kaufmann
Tomasulo Example Cycle 11

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• Write result of ADDD here?
• All quick instructions complete in this cycle!

Tomasulo Example Cycle 15

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• Mult1 (MULTD) completing; what is waiting for it?
Tomasulo Example Cycle 16

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<td></td>
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<td></td>
</tr>
<tr>
<td>4</td>
<td>Mult1</td>
<td>No</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>Mult2</td>
<td>Yes</td>
<td>DIVD</td>
<td>M*F4</td>
<td>R(F6)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Register result status:

<table>
<thead>
<tr>
<th>Clock</th>
<th>F0</th>
<th>F2</th>
<th>F4</th>
<th>F6</th>
<th>F8</th>
<th>F10</th>
<th>F12</th>
<th>...</th>
<th>F30</th>
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<tbody>
<tr>
<td>16</td>
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<td></td>
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<td></td>
</tr>
</tbody>
</table>

Just waiting for Mult2 (DIVD) to complete

Tomasulo Example Cycle 57

Instruction status:

<table>
<thead>
<tr>
<th>Instruction</th>
<th>j</th>
<th>k</th>
<th>Issue</th>
<th>Comp</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD</td>
<td>F6</td>
<td>34+</td>
<td>R2</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>LD</td>
<td>F2</td>
<td>45+</td>
<td>R3</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>MULTD</td>
<td>F0</td>
<td>F2</td>
<td>F4</td>
<td>3</td>
<td>15</td>
</tr>
<tr>
<td>SUBD</td>
<td>F8</td>
<td>F6</td>
<td>F2</td>
<td>4</td>
<td>7</td>
</tr>
<tr>
<td>DIVD</td>
<td>F10</td>
<td>F9</td>
<td>F6</td>
<td>5</td>
<td>56</td>
</tr>
<tr>
<td>ADDD</td>
<td>F6</td>
<td>F8</td>
<td>F2</td>
<td>6</td>
<td>10</td>
</tr>
</tbody>
</table>

Busy Address:

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load1</td>
<td>No</td>
</tr>
<tr>
<td>Load2</td>
<td>Yes</td>
</tr>
<tr>
<td>Load3</td>
<td>No</td>
</tr>
</tbody>
</table>

Reservation Stations:

<table>
<thead>
<tr>
<th>Time</th>
<th>Name</th>
<th>Busy</th>
<th>Op</th>
<th>Vj</th>
<th>Vk</th>
<th>Qj</th>
<th>Qk</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Add1</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Add2</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Add3</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Mult1</td>
<td>No</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>Mult2</td>
<td>Yes</td>
<td>DIVD</td>
<td>M*F4</td>
<td>R(F6)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Register result status:

<table>
<thead>
<tr>
<th>Clock</th>
<th>F0</th>
<th>F2</th>
<th>F4</th>
<th>F6</th>
<th>F8</th>
<th>F10</th>
<th>F12</th>
<th>...</th>
<th>F30</th>
</tr>
</thead>
<tbody>
<tr>
<td>56</td>
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</tr>
</tbody>
</table>

Once again: In-order issue, out-of-order execution and out-of-order completion.
Tomasulo Drawbacks

- **High Complexity** (large circuit, high power consumption)
- Many stores (CDB) at high speed resulting in performance limit by Common Data Bus
  - Each CDB must go to multiple functional units ⇒ high wiring density, high capacitance
  - Number of functional units that can complete per cycle limited to one!
    - Multiple CDBs ⇒ more FU logic for parallel stores
- **Non-precise interrupts!**
  - We will address this later

Tomasulo Loop Example

Loop:
- `LD F0 0 R1`
- `MULTD F4 F0 F2`
- `SD F4 0 R1`
- `SUBI R1 R1 #8`
- `BNEZ R1 Loop`

- This time assume Multiply takes 4 clocks
- Assume 1st load takes 8 clocks (L1 cache miss), 2nd load takes 4 clocks (hit)
- To be clear, will show clocks for SUBI, BNEZ
  - Reality: integer instructions ahead of Fl. Point Instructions
- Show 2 iterations of loop
### Loop Example

**Instruction status:**

<table>
<thead>
<tr>
<th>ITER Instruction</th>
<th>j</th>
<th>k</th>
<th>Issue</th>
<th>Comp</th>
<th>Result</th>
<th>Busy</th>
<th>Addr</th>
<th>Fu</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 LD F0 0 R1</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>No</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1 MULTD F4 F0 F2</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>No</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 SD F4 0 R1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>No</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 LD F0 0 R1</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>No</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>2 MULTD F4 F0 F2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>No</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 SD F4 0 R1</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td>No</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Reservation Stations:**

<table>
<thead>
<tr>
<th>Time</th>
<th>Name</th>
<th>Busy</th>
<th>Op Vj Vk Qj Qk</th>
<th>Code:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Add1</td>
<td>No</td>
<td>LD F0 0 R1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Add2</td>
<td>No</td>
<td>MULTD F4 F0 F2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Add3</td>
<td>No</td>
<td>SD F4 0 R1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Mult1</td>
<td>No</td>
<td>SUBI R1 R1 #8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Mult2</td>
<td>No</td>
<td>BNEZ R1 Loop</td>
<td></td>
</tr>
</tbody>
</table>

**Register result status**

<table>
<thead>
<tr>
<th>Clock</th>
<th>R1</th>
<th>F0 F2 F4 F6 F8 F10 F12 ... F30</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 80</td>
<td></td>
<td>Fu</td>
</tr>
</tbody>
</table>

**Value of Register used for address, iteration control**

---

### Loop Example Cycle 1

**Instruction status:**

<table>
<thead>
<tr>
<th>ITER Instruction</th>
<th>j</th>
<th>k</th>
<th>Issue</th>
<th>Comp</th>
<th>Result</th>
<th>Busy</th>
<th>Addr</th>
<th>Fu</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 LD F0 0 R1</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Yes</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>1 MULTD F4 F0 F2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>No</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 SD F4 0 R1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>No</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Reservation Stations:**

<table>
<thead>
<tr>
<th>Time</th>
<th>Name</th>
<th>Busy</th>
<th>Op Vj Vk Qj Qk</th>
<th>Code:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Add1</td>
<td>No</td>
<td>LD F0 0 R1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Add2</td>
<td>No</td>
<td>MULTD F4 F0 F2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Add3</td>
<td>No</td>
<td>SD F4 0 R1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Mult1</td>
<td>No</td>
<td>SUBI R1 R1 #8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Mult2</td>
<td>No</td>
<td>BNEZ R1 Loop</td>
<td></td>
</tr>
</tbody>
</table>

**Register result status**

<table>
<thead>
<tr>
<th>Clock</th>
<th>R1</th>
<th>F0 F2 F4 F6 F8 F10 F12 ... F30</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 80</td>
<td></td>
<td>Fu</td>
</tr>
</tbody>
</table>

---

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Adapted from UCB and other sources
Loop Example Cycle 2

Instruction status:

<table>
<thead>
<tr>
<th>ITER Instruction</th>
<th>Instruction</th>
<th>Issue</th>
<th>CompResult</th>
<th>Busy</th>
<th>Addr</th>
<th>Fu</th>
</tr>
</thead>
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<tr>
<td>1 LD F0 0 R1</td>
<td>Load1</td>
<td>Yes</td>
<td>80</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 MULTD F4 F0 F2</td>
<td>Load2</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 SD F4 0 R1</td>
<td>Load3</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Store1</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Store2</td>
<td>No</td>
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<tr>
<td></td>
<td>Store3</td>
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Reservation Stations:

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<th>Name</th>
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<th>Op</th>
<th>Vj</th>
<th>Vk</th>
<th>Oj</th>
<th>Ok</th>
<th>Code:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add1</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>F0</td>
</tr>
<tr>
<td>Add2</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>F4</td>
</tr>
<tr>
<td>Add3</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>F0</td>
</tr>
<tr>
<td>Mult1</td>
<td>Yes</td>
<td>Multd</td>
<td>R(F2)</td>
<td>Load1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mult2</td>
<td>No</td>
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</tbody>
</table>

Register result status

<table>
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<tr>
<th>Clock</th>
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<th>F0</th>
<th>F2</th>
<th>F4</th>
<th>F6</th>
<th>F8</th>
<th>F10</th>
<th>F12</th>
<th>...</th>
<th>F30</th>
</tr>
</thead>
<tbody>
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<td>2</td>
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<td>Fu</td>
<td>Load1</td>
<td>Mult1</td>
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</tr>
</tbody>
</table>

ECE568/Koren Part.6.25 Adapted from UCB and other sources Copyright UCB & Morgan Kaufmann

Loop Example Cycle 3

Instruction status:

<table>
<thead>
<tr>
<th>ITER Instruction</th>
<th>Instruction</th>
<th>Issue</th>
<th>CompResult</th>
<th>Busy</th>
<th>Addr</th>
<th>Fu</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 LD F0 0 R1</td>
<td>Load1</td>
<td>Yes</td>
<td>80</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>1 MULTD F4 F0 F2</td>
<td>Load2</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 SD F4 0 R1</td>
<td>Load3</td>
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<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td>Store1</td>
<td>Yes</td>
<td>80 Mult1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Store2</td>
<td>No</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Store3</td>
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<td></td>
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</tbody>
</table>

Reservation Stations:

<table>
<thead>
<tr>
<th>Time</th>
<th>Name</th>
<th>Busy</th>
<th>Op</th>
<th>Vj</th>
<th>Vk</th>
<th>Oj</th>
<th>Ok</th>
<th>Code:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add1</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>F0</td>
</tr>
<tr>
<td>Add2</td>
<td>No</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>F4</td>
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<tr>
<td>Add3</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>F0</td>
</tr>
<tr>
<td>Mult1</td>
<td>Yes</td>
<td>Multd</td>
<td>R(F2)</td>
<td>Load1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mult2</td>
<td>No</td>
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</table>

Register result status

<table>
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<tr>
<th>Clock</th>
<th>R1</th>
<th>F0</th>
<th>F2</th>
<th>F4</th>
<th>F6</th>
<th>F8</th>
<th>F10</th>
<th>F12</th>
<th>...</th>
<th>F30</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>80</td>
<td>Fu</td>
<td>Load1</td>
<td>Mult1</td>
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</tbody>
</table>

* Implicit renaming sets up data flow graph
Loop Example Cycle 4

Instruction status:

<table>
<thead>
<tr>
<th>ITER Instruction</th>
<th>j</th>
<th>k</th>
<th>Issue</th>
<th>CompResult</th>
<th>Busy</th>
<th>Addr</th>
<th>Fu</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD F0 0 R1</td>
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<td>1</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>MULTD F4 F0 F2</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SD F4 0 R1</td>
<td>3</td>
<td></td>
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<td></td>
<td></td>
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</table>

Reservation Stations:

<table>
<thead>
<tr>
<th>Time</th>
<th>Name</th>
<th>Busy</th>
<th>Op</th>
<th>Vj</th>
<th>Vk</th>
<th>Oj</th>
<th>Ok</th>
<th>Code:</th>
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<tbody>
<tr>
<td>Add1</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LD F0 0 R1</td>
</tr>
<tr>
<td>Add2</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MULTD F4 F0 F2</td>
</tr>
<tr>
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<td>SD F4 0 R1</td>
</tr>
<tr>
<td>Mult1</td>
<td>Yes</td>
<td>Multd</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SUBI R1 R1 #8</td>
</tr>
<tr>
<td>Mult2</td>
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<td>BNEZ R1 Loop</td>
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</tbody>
</table>

Register result status

<table>
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<tr>
<th>Clock</th>
<th>R1</th>
<th>F0</th>
<th>F2</th>
<th>F4</th>
<th>F6</th>
<th>F8</th>
<th>F10</th>
<th>F12</th>
<th>...</th>
<th>F30</th>
</tr>
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<tbody>
<tr>
<td>4</td>
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</table>

- Dispatching SUBI Instruction (not in FP queue)

Loop Example Cycle 5

Instruction status:

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<tr>
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<th>j</th>
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<th>Issue</th>
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Reservation Stations:

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<th>Vk</th>
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Register result status

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<th>F12</th>
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- And BNEZ instruction (not in FP queue)
Loop Example Cycle 6

Instruction status:

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Reservation Stations:

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Register result status

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**F0 never sees Load from location 80; no WAW**

Loop Example Cycle 7

Instruction status:

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<th>Fu</th>
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</tr>
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<tr>
<td>SD F4 0 R1</td>
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</tr>
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<td>6</td>
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Reservation Stations:

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<th>Vk</th>
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Register result status

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**Register file completely detached from computation**

**First and Second iteration completely overlapped**
## Loop Example Cycle 8

**Instruction status:**

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<th>Addr</th>
<th>Fu</th>
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<td>MULTD F4 F0 F2</td>
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<td>Load2</td>
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<td>72</td>
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<td>SD F4 0 R1</td>
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<td>LD F0 0 R1</td>
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<td>Store1</td>
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<td>6</td>
<td>80</td>
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<td>MULTD F4 F0 F2</td>
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<td>72</td>
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**Reservation Stations:**

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<td>No</td>
<td>SD F4 0 R1</td>
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<td></td>
<td></td>
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<tr>
<td></td>
<td>Mult1</td>
<td>Yes</td>
<td>Multd R(F2) Load1</td>
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**Register result status**

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<th>F12</th>
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## Loop Example Cycle 9

**Instruction status:**

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<th>Fu</th>
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<td>Load1</td>
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<td>80</td>
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<td>72</td>
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<td>72</td>
<td>Mult2</td>
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**Reservation Stations:**

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<td>Mult2</td>
<td>Yes</td>
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**Register result status**

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<th>F12</th>
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*Load1 completing: who is waiting? Note: Dispatching SUBI*
### Loop Example Cycle 10

**Instruction status:**

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<td>Load2</td>
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<td></td>
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<td>LD F0 0 R1</td>
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<td></td>
<td>Load3</td>
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<td></td>
</tr>
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<td>MULTD F4 F0 F2</td>
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<td>Mult1</td>
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**Reservation Stations:**

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<th>Op</th>
<th>Vj</th>
<th>Vk</th>
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<td>SD F4 0 R1</td>
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<tr>
<td>Mult1</td>
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<td>M[80] R(F2)</td>
<td>SUBI R1 R1 #8</td>
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<td>Mult</td>
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<td>BNEZ R1 Loop</td>
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**Register result status**

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<th>F4</th>
<th>F6</th>
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<th>F10</th>
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♦ Load2 completing: who is waiting? Note: Dispatching BNEZ

### Loop Example Cycle 11

**Instruction status:**

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<th>Issue</th>
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<th>Fu</th>
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♦ Next load in sequence
Loop Example Cycle 12

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Why not issue third multiply?

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Loop Example Cycle 13

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**Reservation Stations:**

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**Register result status**

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Why not issue third store?
Loop Example Cycle 14

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Reservation Stations:  

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♦ Mult1 completing. Who is waiting?

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Loop Example Cycle 15

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♦ Mult2 completing. Who is waiting?
Loop Example Cycle 16

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Reservation Stations:

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<td>BNEZ</td>
<td>R1</td>
<td>R1</td>
<td>#8</td>
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</tr>
</tbody>
</table>

Register result status

<table>
<thead>
<tr>
<th>Clock</th>
<th>R1</th>
<th>F0</th>
<th>F2</th>
<th>F4</th>
<th>F6</th>
<th>F8</th>
<th>F10</th>
<th>F12</th>
<th>...</th>
<th>F30</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>64</td>
<td>Fu</td>
<td>Load3</td>
<td>Mult1</td>
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Loop Example Cycle 17

Instruction status:

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<th>ITER Instruction</th>
<th>j</th>
<th>k</th>
<th>Issue</th>
<th>CompResult</th>
<th>Busy</th>
<th>Addr</th>
<th>Fu</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD F0 0 R1</td>
<td>1</td>
<td>9</td>
<td>10</td>
<td>Load1</td>
<td>No</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MULTD F4 F0 F2</td>
<td>1</td>
<td>14</td>
<td>15</td>
<td>Load2</td>
<td>No</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SD F4 0 R1</td>
<td>1</td>
<td>3</td>
<td>64</td>
<td>Load3</td>
<td>Yes</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>LD F0 0 R1</td>
<td>2</td>
<td>10</td>
<td>11</td>
<td>Store1</td>
<td>Yes</td>
<td>80</td>
<td></td>
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<tr>
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<td>2</td>
<td>15</td>
<td>16</td>
<td>Store2</td>
<td>Yes</td>
<td>72</td>
<td>[72]*R2</td>
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<tr>
<td>SD F4 0 R1</td>
<td>2</td>
<td>8</td>
<td></td>
<td>Store3</td>
<td>Yes</td>
<td>64</td>
<td>Mult1</td>
</tr>
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</table>

Reservation Stations:

<table>
<thead>
<tr>
<th>Time</th>
<th>Name</th>
<th>Busy</th>
<th>Op</th>
<th>Vj</th>
<th>Vk</th>
<th>Qj</th>
<th>Qk</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Add1</td>
<td>No</td>
<td>LD</td>
<td>F0</td>
<td>0</td>
<td>R1</td>
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<td>No</td>
<td>MULTD</td>
<td>F4</td>
<td>F0</td>
<td>F2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Add3</td>
<td>No</td>
<td>SD</td>
<td>F4</td>
<td>0</td>
<td>R1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Mult1</td>
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<td>Multd</td>
<td>R(F2)</td>
<td>Load3</td>
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<td></td>
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<tr>
<td></td>
<td>Mult2</td>
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<td>BNEZ</td>
<td>R1</td>
<td>R1</td>
<td>#8</td>
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</table>

Register result status

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<tr>
<th>Clock</th>
<th>R1</th>
<th>F0</th>
<th>F2</th>
<th>F4</th>
<th>F6</th>
<th>F8</th>
<th>F10</th>
<th>F12</th>
<th>...</th>
<th>F30</th>
</tr>
</thead>
<tbody>
<tr>
<td>17</td>
<td>64</td>
<td>Fu</td>
<td>Load3</td>
<td>Mult1</td>
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</tr>
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</table>
### Loop Example Cycle 18

**Instruction status:**

<table>
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<tr>
<th>ITER Instruction</th>
<th>j</th>
<th>k</th>
<th>Issue</th>
<th>CompResult</th>
<th>Busy</th>
<th>Addr</th>
<th>Fu</th>
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</thead>
<tbody>
<tr>
<td>1 LD F0 0 R1</td>
<td>1</td>
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<td>10</td>
<td>Load1</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>1 MULTD F4 F0 F2</td>
<td>2</td>
<td>14</td>
<td>15</td>
<td>Load2</td>
<td>No</td>
<td></td>
<td></td>
</tr>
<tr>
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<td></td>
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<td>11</td>
<td>Store1</td>
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<td>80</td>
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<td>15</td>
<td>16</td>
<td>Store2</td>
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<td>72</td>
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<tr>
<td>2 SD F4 0 R1</td>
<td>8</td>
<td>19</td>
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<td>Store3</td>
<td>Yes</td>
<td>64</td>
<td>Mult1</td>
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</tbody>
</table>

**Reservation Stations:**

<table>
<thead>
<tr>
<th>Time</th>
<th>Name</th>
<th>Busy</th>
<th>Op</th>
<th>Vj</th>
<th>Vk</th>
<th>Qj</th>
<th>Qk</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add1</td>
<td>No</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>Mult1</td>
<td>Yes</td>
<td>Multd</td>
<td>R(F2)</td>
<td>Load3</td>
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<td>Mult2</td>
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**Register result status**

<table>
<thead>
<tr>
<th>Clock</th>
<th>R1</th>
<th>F0</th>
<th>F2</th>
<th>F4</th>
<th>F6</th>
<th>F8</th>
<th>F10</th>
<th>F12</th>
<th>...</th>
<th>F30</th>
</tr>
</thead>
<tbody>
<tr>
<td>18</td>
<td>64</td>
<td>Fu</td>
<td>Load3</td>
<td>Mult1</td>
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</tr>
</tbody>
</table>
Loop Example Cycle 20

### Instruction status:

<table>
<thead>
<tr>
<th>ITER</th>
<th>Instruction</th>
<th>j</th>
<th>k</th>
<th>Issue</th>
<th>CompResult</th>
<th>Busy</th>
<th>Addr</th>
<th>Fu</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LD F0 0 R1</td>
<td>1</td>
<td>9</td>
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<td>Load1</td>
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</tr>
<tr>
<td>1</td>
<td>MULTD F4 F0 F2</td>
<td>2</td>
<td>14</td>
<td>15</td>
<td>Load2</td>
<td>No</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>SD F4 0 R1</td>
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<td>18</td>
<td>19</td>
<td>Load3</td>
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<tr>
<td>2</td>
<td>LD F0 0 R1</td>
<td>6</td>
<td>10</td>
<td>11</td>
<td>Store1</td>
<td>No</td>
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</tr>
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<td>MULTD F4 F0 F2</td>
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<td>15</td>
<td>16</td>
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<tr>
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<td>SD F4 0 R1</td>
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<td>20</td>
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<td>Yes</td>
<td>64</td>
<td>Mult1</td>
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</tbody>
</table>

### Reservation Stations:

<table>
<thead>
<tr>
<th>Time</th>
<th>Name</th>
<th>Busy</th>
<th>Op</th>
<th>Vj</th>
<th>Vk</th>
<th>Qj</th>
<th>Qk</th>
<th>Code:</th>
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<tr>
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<td>MULTD F4 F0 F2</td>
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<tr>
<td></td>
<td>Add3</td>
<td>No</td>
<td>SD F4 0 R1</td>
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<tr>
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<td>Mult1</td>
<td>Yes Multd</td>
<td>SUBI R1 R1 #8</td>
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<tr>
<td></td>
<td>Mult2</td>
<td>No</td>
<td>BNEZ R1 Loop</td>
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</table>

### Register result status

<table>
<thead>
<tr>
<th>Clock</th>
<th>R1</th>
<th>F0</th>
<th>F2</th>
<th>F4</th>
<th>F6</th>
<th>F8</th>
<th>F10</th>
<th>F12</th>
<th>...</th>
<th>F30</th>
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<tbody>
<tr>
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</tbody>
</table>

- In-order issue, out-of-order execution & completion across loop iterations

---

Why can Tomasulo overlap iterations of loops?

- **Register renaming**
  - Multiple iterations use different physical destinations for registers (dynamic loop unrolling)

- **Reservation stations**
  - Permit instruction issue to advance past integer control flow operations
  - Also buffer old values of registers - totally avoiding the WAR stall that we saw in the scoreboard

- **Other perspective: Tomasulo building data flow dependency graph on the fly**
Summary: Tomasulo’s scheme offers two major advantages

(1) The distribution of the hazard detection logic
   - distributed reservation stations and the CDB
   - If multiple instructions waiting on single result, & each instruction has the other operand, then instructions can be released simultaneously by broadcast on CDB
   - If a centralized register file were used, the units would have to read their results from the registers when register buses are available

(2) The elimination of stalls for WAW and WAR hazards